

ML4024

MSA Compliant

SFP28 MCB



Revision 0.5



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1. General description

SFP28 Host (Small Form Factor 28) MSA Compliant Host board ML4024, is designed to provide an efficient and easy method of programming and testing 28G SFP28 transceivers.

The SFP28 host is designed to simulate an ideal environment for SFP28 transceivers module and cable testing, characterization and manufacturing tests. Its properties make the host board as electrically transparent as possible, allowing for a more accurate assessment of the module's performance.

2. ML4024 SFP host test board – Key Features

- ✓ DUT voltage supply control (3.15V, 3.3V, 3.45V)
- ✓ DUT Current Sense
- ✓ Superior Signal Integrity Performance Rogers 3003 based PCBs
- ✓ Low Insertion Loss
- ✓ Temperature Monitor
- ✓ Four corner test capability
- ✓ Supports 28G interfaces
- ✓ TX and RX channels come with matching trace length
- ✓ I2C master driven from both on board micro controller or external pin headers
- ✓ USB interface
- ✓ User friendly GUI for I2C R/W commands and loading custom MSA Memory Maps
- ✓ On-board LEDs showing MSA output Alarms states
- ✓ On-board buttons/jumpers for MSA input control signals
- ✓ 2.92mm 40GHz edge launch k connectors



3. Operating Conditions

Recommended Operation Conditions								
Parameter	Symbol	Notes/Conditions	Min	Тур	Max	Units		
Operating Temperature	Тд		0		85	°C		
Supply Voltage	VCC	Main Supply Voltage		3.3		V		
Data Rate	Rb	Guaranteed to work at 28 Gbps per lane	0		28	Gbps		

3.1 LEDs

The LED D1 indicates whether a USB cable is plugged or not.

The other two LEDs, D2 and D4, are used for diagnostic purposes.

- If the green LED, D2, is on: USB is locked and device is recognized by the USB driver.
- If the red LED, D4, is on: USB not connected or USB driver not found.
- If both LEDs are off: Board not powered correctly or firmware is corrupted.

4. Power Supplies

The board can be powered using a 3.3V external power supply via a female AMP connector, PN: A103942-ND.

However, an additional 5V power supply can be used in case the variable VCC (3.15V, 3.3V or 3.45V) feature is needed. In this case, R5 must be populated and R3 must not be populated. (Figure 1)



Figure 1: K3 and K5

A current sense is available on the board, and it measures the current draw on the main P3V3 net.



5. SFP HW Signaling Pins

Hardware alarm pins, hardware control pins and I2C pins can be accessed from the software via USB or through on-board LEDs and pin headers.

5.1 Alarms signals

The hardware alarm signals (RX_LOS, MOD_ABS and TX_FAULT) can be accessed from the pin headers as shown in figure 2 or from the LEDs as shown in figure 3.



Figure 2: Alarms pins



Figure 3: Alarms LEDs

5.2 Controls signals

The hardware control signals (RATESELO, RATESEL1 and TXDISABLE) can be accessed using jumpers as shown in figure 4. Note that a jumper needs to be used on HW_CNTRL to release the pins from the microcontroller and enable the access from on board jumpers.

multiLane



Figure 4: Control pins

5.3 I2C pins

The I2C pins SCL and SDA can be accessed via jumpers as shown in figure 5. Note that a jumper needs to be used on HW_I2C to release the pins from the microcontroller and enable the access from on board pin headers.



Figure 5: I2C HW pins



6. The SFP Graphical User Interface

6.1 Communication Window

This is the main interface used for initial communication with the host.

MainWindow		×
multiLane	Communication	-
SFP Host	USB instance: 0 Disconnect Refresh Pause Monitor About Us Connected to Host Board Firmware Info: Device ID : 0 FW Rev. : 1 USB Connected USB Error USB Error	und I

Figure 6: Communication window

The Initialize button is the application's main entry point, used to establish a connection with the SFP Host board and the Module. Once a USB connection is established, the Host checks if a SFP Module is inserted, and accordingly illuminates the corresponding (*Module Found* or *Module Not Found*) LED. And when the USB connection is lost, the USB Error LED is illuminated.

The status box window in the GUI will show any success or failure messages that are being returned as a result of the GUI communicating or attempting to communicate with the hardware.

- *Refresh* button: checks for connection status, refresh Hardware Readings and updates GUI.
- Pause Monitor button: Pause/Resume monitoring.
- About Us button: shows program information (name, version) and company information.

Note that multiple boards can be connected via USB. The desired board is selected using USB Instance field from the *Communication* window.



6.2 Monitor tab

This tab is the main source of the module status and alarm/warning flags conditions. It shows the current status of a flag, as defined in the SFF-8472.

larms	Warnings	Measurements		
High Low TX Pwr TX Bias Vcc RX Pwr Op Lsr T* Op TEC C	High Low Tx Pwr Tx Bias Vcc Temp Rx Pwr Op Lsr T* Op TEC C	Tx Pwr Tx Bias Vcc Temp Rx Pwr Op Lsr T [*] Op TEC C	mW uA V °C mW °C mA	
ost Current Sense				

Figure 7: Monitor tab



ine diditi	is and w	varnings are defined in slav	
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
	5	Optional Laser Temp High Alarm	Set when laser temperature or wavelength exceeds the high alarm level.
	4	Optional Laser Temp Low Alarm	Set when laser temperature or wavelength is below the low alarm level.
	3	Optional TEC current High Alarm	Set when TEC current exceeds the high alarm level.
	2	Optional TEC current Low Alarm	Set when TEC current is below the low alarm level.
	1	Reserved Alarm	
	0	Reserved Alarm	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
	6	Temp Low Warning	Set when internal temperature is below low warning level.
	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
	4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
	1	TX Power High Warning	Set when TX output power exceeds high warning level.
	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.
	6	RX Power Low Warning	Set when Received Power is below low warning level.
-			

The alarms and warnings are defined in slave address A2h, bytes 112, 113, 116 and 117 as below:

Figure 8: Alarm and warning flag bits (from SFF-8472)

And the following are the A/D values (measurements) [Address A2h, Bytes 96-109]:

multiLane

A2	Bit	Name	Description
Conv	erted	analog values. Calibrated	d 16 bit data.
96	All	Temperature MSB	Internally measured module temperature.
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver.
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias Current.
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power.
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power.
105	All	RX Power LSB	
106	All	Optional Laser Temp/Wavelength MSB	Measured laser temperature or wavelength
107	All	Optional Laser Temp/Wavelength LSB	
108	All	Optional TEC current MSB	Measured TEC current (positive is cooling)
109	All	Optional TEC current LSB	

Figure 9: A/D values and status bits

Measurements calculations:

Temp: Internally measured transceiver temperature. Represented as a 16 bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of -128C to +128C. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over specified operating temperature and voltage. (Ref. SFF-8472)

Vcc: Internally measured transceiver supply voltage. Represented as a 16 bit unsigned integer with the voltage defined as the full 16 bit value (0-65535) with LSB equal to 100 uVolt, yielding a total range of 0 to +6.55 Volts. Practical considerations to be defined by transceiver manufacturer will tend to limit the actual bounds of the supply voltage measurement. (Ref. SFF-8472)

Tx Bias: Measured TX bias current in uA. Represented as a 16 bit unsigned integer with the current defined as the full 16 bit value (0-65535) with LSB equal to 2 uA, yielding a total range of 0 to 131 mA. (Ref. SFF-8472)

Tx Pwr: Measured TX output power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0-65535) with LSB equal to 0.1 uW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). (Ref. SFF-8472)

Rx Pwr: Measured RX received optical power in mW. Value can represent either average received power or OMA depending upon how bit 3 of byte 92 (A0h) is set. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0-65535) with LSB equal to 0.1 uW, yielding a total range of 0 to 6.5535 mW (\sim -40 to +8.2 dBm). (Ref. SFF-8472)



Op Lsr T°: Measured optional laser temperature. The encoding is the same as for transceiver internal temperature defined above (**Temp**). (Ref. SFF-8472)

Op TEC C: Measured TEC current. The format is signed two's complement with the LSB equal to 0.1 mA. Thus a range from -3276.8 to +3276.7 mA may be reported with a resolution of 0.1 mA. Reported TEC current is a positive number for cooling and a negative number for heating. (Ref. SFF-8472)

6.3 SFF8419 tab

This tab shows the Low Speed Electrical Control Contacts.

Module Output	Module Input
Tx_Fault	Tx_Disable
Mod_ABS	Rate Select HW Control Contacts
Rx_LOS	RS0
Refresh	🔲 RS1

Figure 10: SFF8419 tab

6.3.1 TX_Fault

Tx_Fault is a module output that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety. (Ref. SFF-8419)

6.3.2 Mod_ABS

Mod_ABS is connected to VeeT or VeeR in the SFP+ module. It is asserted 'High' when the SFP+ module is physically absent from a host slot. (Ref. SFF-8419)

6.3.3 Rx_LOS

Rx_LOS when high indicates an optical signal level below that specified in the relevant standard. (SFF-8419)

6.3.4 Tx_Disable

When Tx_Disable is asserted high or left open, the SFP+ module transmitter output shall be turned off unless the module is a passive cable assembly in which case this signal may be ignored. (Ref. SFF-8419)



6.3.5 RS0/RS1

RSO and RS1 are module inputs and are pulled low to VeeT with >30 kOhms resistors in the module. RSO optionally selects the optical receive signaling rate coverage.

RS1 optionally selects the optical transmit signaling rate coverage. (Ref. SFF-8419)

6.4 Controls tab

This tab displays the optional status/control bits.

Status Bits	Control Bits	
TX Disable State	Soft TX Disable Select	
O RS(1) State	Soft RS(0) Select	
C RS(0) State		
○ TX Fault State		
RxLOS State		
DataReady_Bar State		

Figure 11: Controls tab



These bits are defined in the SFF8472 in register 110:

110	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100ms of change on pin.
	6	Soft TX Disable Select	Read/write bit that allows software disable of laser. Writing '1' disables laser. See Table 8-7 for enable/disable timing requirements. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is zero/low.
	5	RS(1) State	Digital state of SFP input pin AS(1) per SFF-8079 or RS(1) per SFF-8431. Updated within 100ms of change on pin. See A2h Byte 118, Bit 3 for Soft RS(1) Select control information.
5	4	Rate_Select State [aka. "RS(0)"]	Digital state of the SFP Rate_Select Input Pin. Updated within 100ms of change on pin. Note: This pin is also known as AS(0) in SFF-8079 and RS(0) in SFF-8431.
	3	Soft Rate_Select Select [aka. "RS(0)"]	Read/write bit that allows software rate select control. Writing '1' selects full bandwidth operation. This bit is "OR'd with the hard Rate_Select, AS(0) or RS(0) pin value. See Table 8-7 for timing requirements. Default at power up is logic zero/low, unless specifically redefined by value selected in Table 5-6. If Soft Rate Select is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 5-6 and referenced documents. See Table 10-1, byte 118, bit 3 for Soft RS(1) Select.
Ī	2	TX Fault State	Digital state of the TX Fault Output Pin. Updated within 100ms of change on pin.
	1	Rx_LOS State	Digital state of the RX_LOS Output Pin. Updated within 100ms of change on pin.
	0	Data_Ready_Bar State	Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.

Figure 12: Optional Status/Control bits

6.5 I2C R/W tab

This tab allows the user to read from the memory and write to it.



. Select a slave address	2. Select a memory page	
A0h A2h Other A0 h Set	 Page 00 Page 01 Page 00 	O Page 02 O Other
le byte - I2C Read/Write	Multi-Byte - Read/Write	
ter register address: (Dec) Oec Disp. Hex Disp.	From address To address (Decimal) (Decimal)	Read
ter the value to be written: (Hex) O Dec Disp. Hex Disp.	Address	Value (Hex)



In order to access a register in the memory:

- 1. Select a slave address from the *Slave Address* window (by default A0h is selected).
- 2. Select the desired memory page from the *Memory Location* window (by default Page00 is selected).
- 3. Go to *Single byte-I2C Read/Write* window in case you need to access one register address only, otherwise, discard that window and go to the *Multi Byte Read/Write* window.

Note that:

- The *Read* button reads the memory content of the desired register address(es).
- The *Write* and *Save* buttons write the desired register values to the SFP module.



6.6 Bulk I2C R/W tab

This tab allows the user to load or save his custom SFP configuration.

	2C R/W Bulk I2C R/W	Base ID Extend	ed ID		
Choose addresses to display:	Read	Save MSA to file			
Slave address A0 🔹	Write to HW	Load MSA from file			
Address	Data (Hex)	Data (Dec)	Data (Ascii)	MSA Description	
S.A. A0 Byte 0 (00h)	00	00		Serial ID	
S.A. AD Byte 1 (01h)	00	00		Serial ID	Ĩ
5.A. A0 Byte 2 (02h)	00	00		Serial ID	
S.A. AO Byte 3 (O3h)	00	00		Serial ID	
S.A. AO Byte 4 (O4h)	00	00		Serial ID	
S.A. A0 Byte 5 (05h)	00	00		Serial ID	l l
S.A. A0 Byte 6 (06h)	00	00		Serial ID	
S.A. A0 Byte 7 (07h)	00	00		Serial ID	
S.A. AO Byte 8 (O8h)	00	00		Serial ID	
S.A. AD Byte 9 (09h)	00	00		Serial ID	Ĵ
S.A. AO Byte 10 (OAh)	00	00		Serial ID	
S.A. AD Byte 11 (OBh)	00	00		Serial ID	
S.A. AD Byte 12 (OCh)	00	00		Serial ID	
S.A. AD Byte 13 (ODh)	00	00		Serial ID	
5.A. A0 Byte 14 (0Eh)	00	00		Serial ID	
S.A. AO Byte 15 (OFh)	00	00		Serial ID	
S.A. AD Byte 16 (10h)	00	00		Serial ID	

Figure 14: Bulk I2C R/W tab

- *Read* button: Reads the content of the SFP MSA registers of the selected Slave Address (S.A.) and refreshes the grid.
- *Write to HW* button: Writes the displayed MSA configuration to the SFP module.
- Save MSA to file button: Saves the current MSA memory to a file using CSV (comma separated values) format.
- Load MSA from file button: Loads MSA values from a file and map it to MSA memory.



6.7 Base ID tab

This tab displays the identifiers. It refers to the SFF-8472, and is presented without any modification or change. The targeted information is read from the correspondent registers, calculated or enumerated when required, and presented to the user on the screen (figure 18) in a simple readable ASCII format.

Refresh page	Transceiver	
Nodule Identifier	10GE Co C	Vendor Name
Ext. Identifier	Infiniband Co	Vendor OUI
Connector	ESCON Co C	Vendor PN
incoding	SONET Co C	Vendor rev
3R, Nominal	Ethernet Co C	Wavelength
late identifier	Fibre Channel Link Length	
ength (SMF, km)	Fibre Channel Technologie	
ength (SMF)	SFP+ Cable Tech	
ength (50um)	Fibre Channel Transmission Media	
ength (62.5um)	Fibre Channel Speed	
ength (OM4 or opper cable)		CC_BASE
ength (OM3)	Co C: Compliance	Codes CC_BASE Calculated

Figure 15: Base ID tab

The check code (CC_BASE) is a one byte code that can be used to verify that the first 64 bytes of twowire interface information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 0 to byte 62, inclusive.



6.8 Extended ID tab

This tab display link characteristics.

Refresh page	Option Values	Enhanced Options
R, max	High Power Level Declaration. Paging implemented indicator.	Optional Alarm/warning flags implemented for all monitored quantities.
endor SN	Retimer or CDR indicator.	Optional soft TX_DISABLE control and monitoring implemented.
F-8472	Power Level Declaration.	Optional soft TX_FAULT monitoring implemented.
endor Specific EPROM	Linear Receiver Output Implemented.	Optional soft RATE_SELECT control and monitoring implemented.
Diagnostic Monitoring Type Reserved for legacy diagnostic implementations. Must be '0' for	Tunable transmitter technology. RATE_SELECT functionality is implemented.	Optional soft RX_LOS monitoring implemented.
compliance with SFF-8472. Digital diagnostic monitoring implemented (described in this	TX_DISABLE is implemented and disables the high speed serial output.	Optional Application Select control implemented per SFF-8079.
document). Must be 'l' for compliance with this document.	TX_FAULT signal implemented.	Optional soft Rate Select control implemented per SFF-8431.
) Internally calibrated.) Externally calibrated.	Loss of Signal implemented (Rx_LOS).	
Received power measurement type 0 = OMA, 1 = average power.	Bit value is 0 🛛 🖲 Bit value is 1	CC_EXT Calculated



The check code (CC_EXT) is a one byte code that can be used to verify that the first 32 bytes of extended two-wire interface information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive.



Revision History

Revision number	Description	Date
0.1	Preliminary	29/09/2015
0.2	Added power cable connector name	05/11/2015
0.3	Added USB instance	24/08/2016
0.4	Туро	12/10/2016
0.5	Updated ML4024 picture	05/09/2017