multiLane

ML4064-ALB2-112

Technical Reference

OSFP Electrical Active Loopback Module

CMIS 5.0 Compliant

Innovation for the next generation

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1 Overview

The **ML4064-ALB2-112** is an OSFP active electrical loopback module that provides a straightforward method to test OSFP ports at every level of the switch production process.
The active electrical loopback (ALB) includes a transceiver chip, where 8xTX channels and 8xRX channels are available. Data is transmitted from the host to the TX input port of the active loopback, and the retimed signal is received by the host via the RX output port of the active loopback. The **ML4064-ALB2-112** is ideal for R&D validation, production testing, and field testing. The **ML4064-ALB2-112** follows the **CMIS Rev 5.0** standard and is packaged in standard MSA housing compatible with all OSFP power classes.

1.1 ML4064-ALB2-112 OSFP active loopback | Key Features

- OSFP MSA Form Factor
- MSA Compatible Configuration and EEPROM
- Programmable MSA memory pages
- Custom memory maps
- I2C Interface
- USB Interface
- Electrical transceiver chip
- Separate daughter card for power spots
- Additional programmable power heaters, dissipating up to 19W
- Two temperature sensors
- Voltage sensor
- Cut-off temperature preventing module overheating

1.2 Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		-40		85	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.6	V
Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω

2 Management Data Interface – I2C

The **ML4064-ALB2-112** supports the I2C interface.

2.1 I2C Signals, Addressing and Frame Structure

2.1.1 I2C Frame

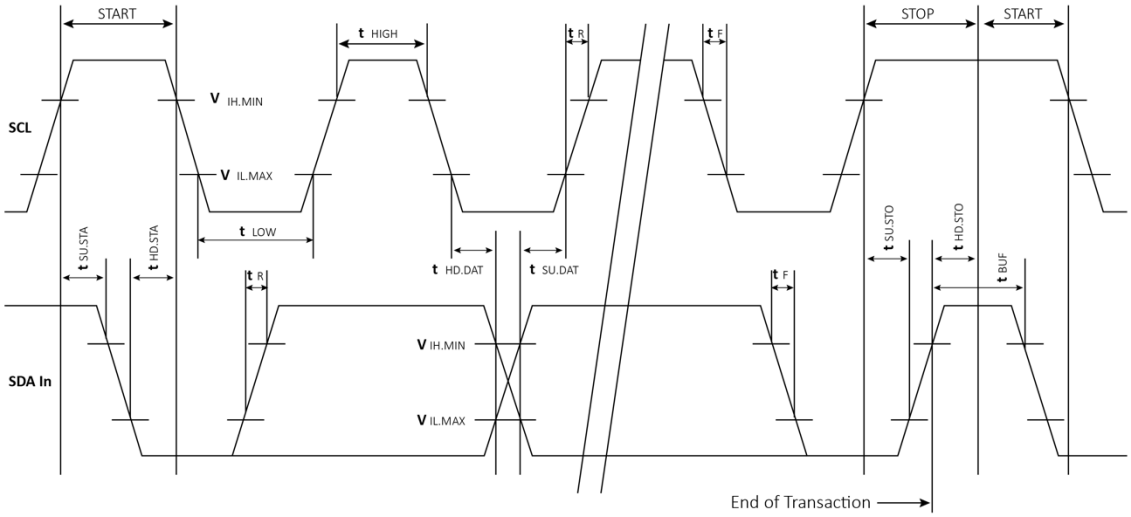

Figure 1: OSFP Timing Diagram

2.1.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the OSFP module are shown in the table below:

Parameter	Symbol	Min	Max	Unit
Clock Frequency	f_{SCL}	10	1015	kHz
Clock Pulse Width Low	t_{LOW}	0.35		us
Clock Pulse Width High	t_{High}	0.35		us
Time bus free before new transmission can start	t_{BUF}	1.5		us
START Hold Time	$t_{HD.STA}$	0.08		us
START Set-up Time	$t_{SU.STA}$	0.4		us
Data In Hold Time	$t_{HD.DAT}$	0.1		us
Data in Set-up Time	$t_{SU.DAT}$	0.1		us
STOP Set-up Time	$t_{SU.STO}$	0.4		us

Parameter	Symbol	Min	Max	Unit
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold		125	us
Complete Single Write	tWR		40	ms

Maximum time the OSFP Module may hold the SCL line low before continuing with a read or write operation is 500us.

2.1.3 Device Addressing and Operation

Serial Clock (SCL): The host supplied SCL input to OSFP transceivers is used to positive-edge clock data into each OSFP device and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain or open-collector driven.

Master/Slave: OSFP transceivers operate only as slave devices. The host must provide a bus master for SCL and initiate all read/write communication.

Device Address: Each OSFP is hard wired at the device address A0h.

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicating a START or STOP condition. All addresses and data words are serially transmitted to and from the OSFP in 8-bit words. Every byte on the SDA line must be 8-bit long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one-bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word. Device address bytes and write data bytes initiated by the host are acknowledged by OSFP transceivers. Read data bytes transmitted by OSFP transceivers should be acknowledged by the host for all but the final byte read, for which the host should respond with a STOP instead of an ACK.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the OSFP management interface can be reset. Memory reset is intended only to reset the OSFP transceiver management interface (to correct a hung bus). No other transceiver functionality is implied.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: OSFP devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 1. This is common to all OSFP devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 1: OSFP Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address the OSFP transceiver output a zero (ACK) on the SDA line to acknowledge the address.

2.2 OSFP Memory Map

2.2.1 Full Map

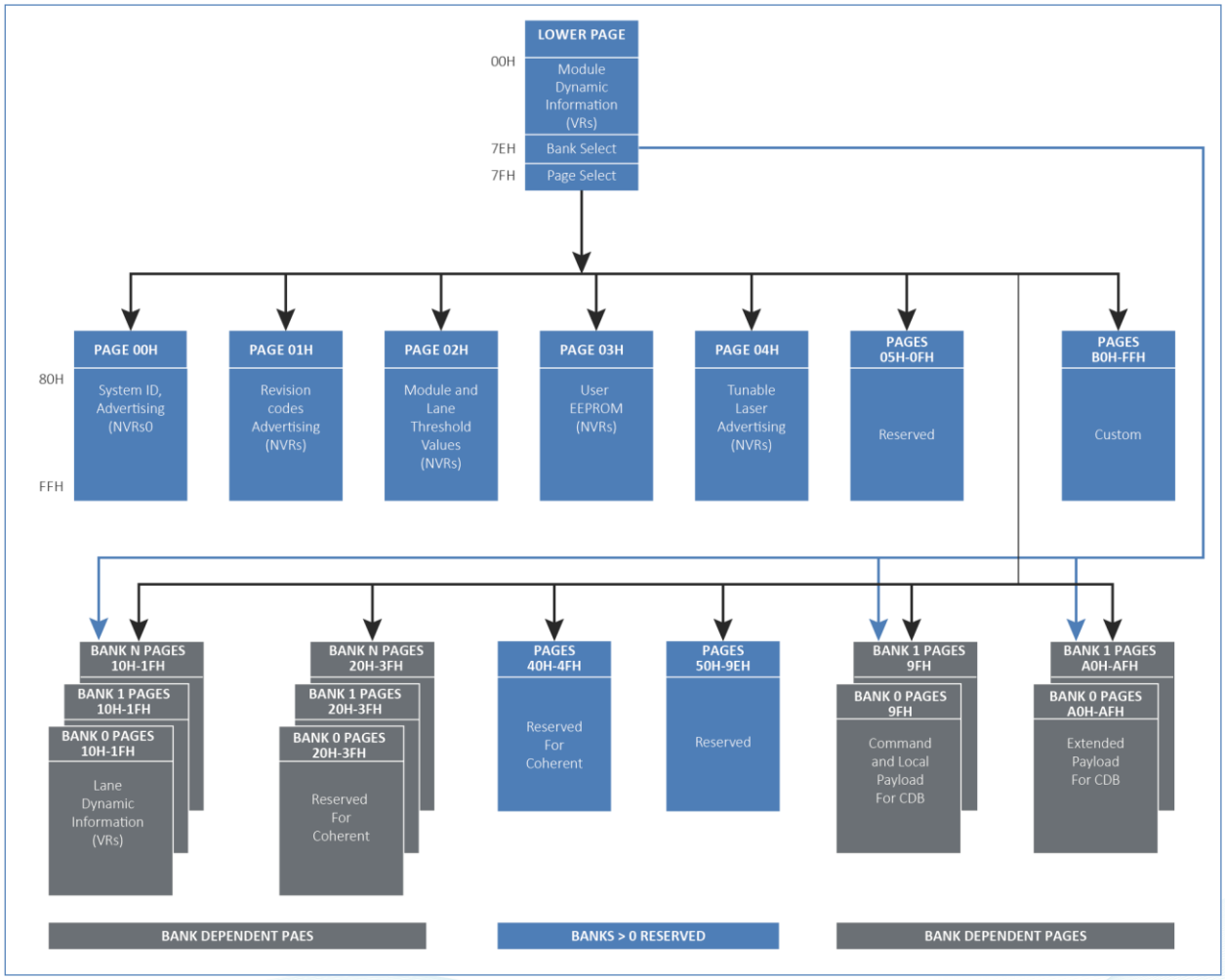

Figure 3: OSFP Memory Map

This section defines the Memory Map for OSFP transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all OSFP devices.
The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

2.2.2 ML4064-ALB2-112 Memory Map

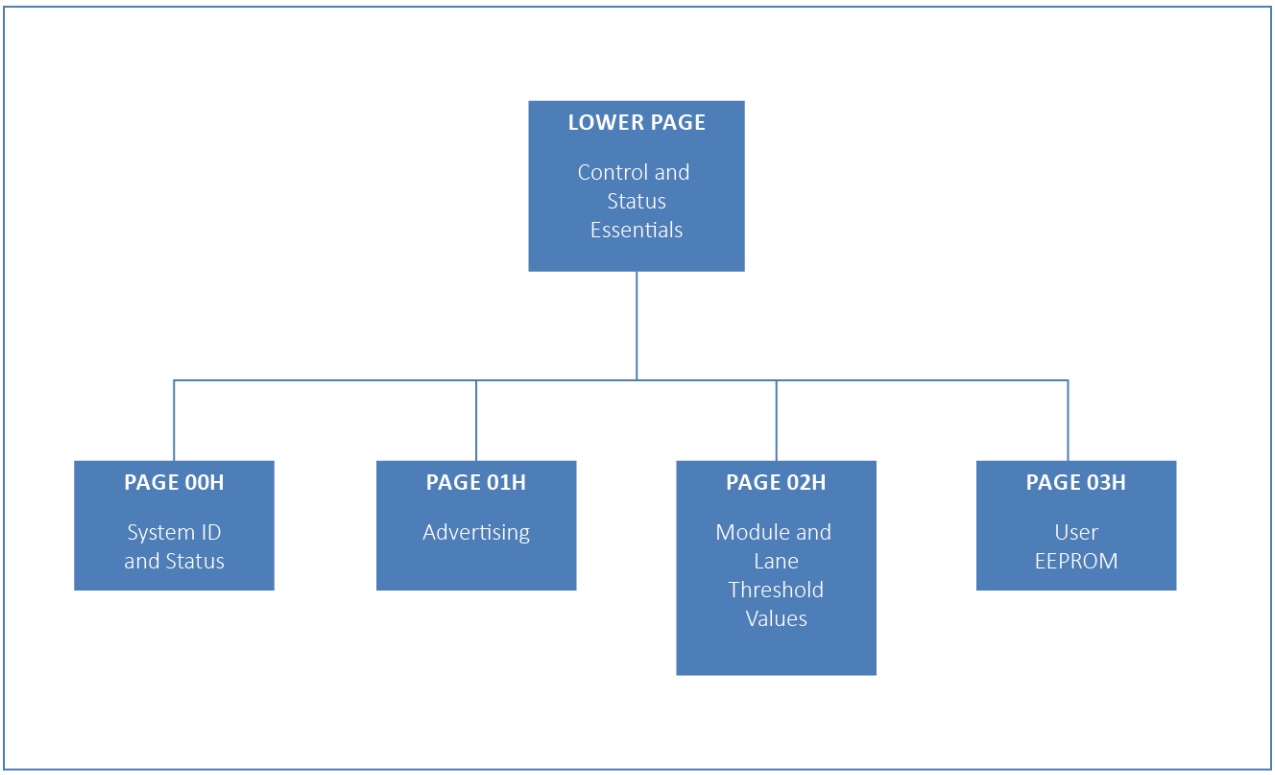

Figure 4: Implemented Memory Map

2.2.3 Memory Content

The table below shows the memory content.

Address	Hex	Decimal	ASCII	MSA Description
LowMem 0(00h)	0x19	24		Identifier
LowMem 1(01h)	0x50	80	P	Revision Compliance
LowMem 2(02h)	0x00	0		Flat-mem / TWI Max Speed
LowMem 3(03h)	0x06	6		Module State / Software interrupt
LowMem 4(04h)	0x00	0		Bank 0 flag summary
LowMem 5(05h)	0x00	0		Bank 1 flag summary

LowMem 6(06h)	0x00	0		Bank 2 flag summary
LowMem 7(07h)	0x00	0		Bank 3 flag summary
LowMem 8(08h)	0x00	0		Data Path/Module FW fault and Module State changed flag
LowMem 9(09h)	0x00	0		Latched VCC3.3/Temp Alarm and Warning
LowMem 10(0Ah)	0x00	0		Latched AUX1/2 Alarm and Warning
LowMem 11(0Bh)	0x00	0		Latched Vendor Defined/AUX3 Alarm and Warning
LowMem 12(0Ch)	0x00	0		Reserved
LowMem 13(0Dh)	0x00	0		Custom
LowMem 14(0Eh)				Internally measured Temperature T.S.1 MSB
LowMem 15(0Fh)				Internally measured Temperature T.S.1 LSB
LowMem 16(10h)				Internally measured Supply 3.3v MSB
LowMem 17(11h)				Internally measured Supply 3.3v LSB
LowMem 18-23 (12h-17h)	0x00	0		
LowMem 24(18h)				Transceiver Internally measured Temperature MSB
LowMem 25(19h)				Transceiver Internally measured Temperature LSB
LowMem 26(1Ah)	0x40	64	@	Software reset / Low power control
LowMem 27-38 (1Bh-26h)	0x00	0		
LowMem 39(27h)	0x01	1		Major FW Rev
LowMem 40(28h)	0x01	1		Minor FW Rev
LowMem 41-84 (29h-54h)	0x00	0		
LowMem 85(55h)	0x04	4		Media Type
LowMem 86(56h)	0x51			Host Interface ID AppSel code 1
LowMem 87(57h)	0xBF			Media Interface ID AppSel code 1
LowMem 88(58h)	0x88			Host and Media Lane Count AppSel code 1
LowMem 89(59h)	0x01			Host Lane Assignment Options AppSel code 1
LowMem 90(5Ah)	0x4F			Host Interface ID AppSel code 2
LowMem 91(5Bh)	0xBF			Media Interface ID AppSel code 2
LowMem 92(5Ch)	0x88			Host and Media Lane Count AppSel code 2
LowMem 93(5Dh)	0x01			Host Lane Assignment Options AppSel code 2
LowMem 94-125 (5Eh-7Dh)	0x00	0		

LowMem 126(7Eh)	0x00	0		Bank Select Byte
LowMem 127(7Fh)	0x00	0		Page Select Byte
Page00 128(80h)	0x19	25		Identifier
Page00 129(81h)	0x4D	77	M	Vendor Name
Page00 130(82h)	0x55	85	U	Vendor Name
Page00 131(83h)	0x4C	76	L	Vendor Name
Page00 132(84h)	0x54	84	T	Vendor Name
Page00 133(85h)	0x49	73	I	Vendor Name
Page00 134(86h)	0x4C	76	L	Vendor Name
Page00 135(87h)	0x41	65	A	Vendor Name
Page00 136(88h)	0x4E	78	N	Vendor Name
Page00 137(89h)	0x45	69	E	Vendor Name
Page00 138(8Ah)	0x20	32		Vendor Name
Page00 139(8Bh)	0x20	32		Vendor Name
Page00 140(8Ch)	0x20	32		Vendor Name
Page00 141(8Dh)	0x20	32		Vendor Name
Page00 142(8Eh)	0x20	32		Vendor Name
Page00 143(8Fh)	0x20	32		Vendor Name
Page00 144(90h)	0x20	32		Vendor Name
Page00 145(91h)	0x00	0		Vendor OUI
Page00 146(92h)	0x00	0		Vendor OUI
Page00 147(93h)	0x00	0		Vendor OUI
Page00 148(94h)	0x34	52	4	Vendor PN
Page00 149(95h)	0x30	48	0	Vendor PN
Page00 150(96h)	0x36	54	6	Vendor PN
Page00 151(97h)	0x34	48	4	Vendor PN
Page00 152(98h)	0x41	65	A	Vendor PN
Page00 153(99h)	0x4C	76	L	Vendor PN
Page00 154(9Ah)	0x42	66	B	Vendor PN
Page00 155(9Bh)	0x32	50	2	Vendor PN

Page00 156(9Ch)	0x2D	45	-	Vendor PN
Page00 157(9Dh)	0x31	45	1	Vendor PN
Page00 158(9Eh)	0x31	79	1	Vendor PN
Page00 159(9Fh)	0x32	83	2	Vendor PN
Page00 160(A0h)	0x20	32		Vendor PN
Page00 161(A1h)	0x20	32		Vendor PN
Page00 162(A2h)	0x20	32		Vendor PN
Page00 163(A3h)	0x20	32		Vendor PN
Page00 164(A4h)	0x01	1		Vendor Rev
Page00 165(A5h)	0x00	0		Vendor Rev
Page00 166(A6h)	0x20	32		Vendor SN
Page00 167(A7h)	0x20	32		Vendor SN
Page00 168(A8h)	0x20	32		Vendor SN
Page00 169(A9h)	0x20	32		Vendor SN
Page00 170(AAh)	0x20	32		Vendor SN
Page00 171(ABh)	0x20	32		Vendor SN
Page00 172(ACh)	0x20	32		Vendor SN
Page00 173(ADh)	0x20	32		Vendor SN
Page00 174(AEh)	0x20	32		Vendor SN
Page00 175(AFh)	0x20	32		Vendor SN
Page00 176(B0h)	0x20	32		Vendor SN
Page00 177(B1h)	0x02	32		Vendor SN
Page00 178(B2h)	0x20	32		Vendor SN
Page00 179(B3h)	0x20	32		Vendor SN
Page00 180(B4h)	0x20	32		Vendor SN
Page00 181(B5h)	0x20	32		Vendor SN
Page00 182(B6h)	0x32	50	2	Date Code
Page00 183(B7h)	0x31	49	1	Date Code
Page00 184(B8h)	0x30	48	0	Date Code
Page00 185(B9h)	0x35	53	5	Date Code

Page00 186(BAh)	0x32	50	2	Date Code
Page00 187(BBh)	0x37	55	7	Date Code
Page00 188(BCh)	0x30	48	0	Date Code
Page00 189(BDh)	0x31	49	1	Date Code
Page00 190(BEh)	0x00	0		CLEI Code
Page00 191(BFh)	0x00	0		CLEI Code
Page00 192(C0h)	0x00	0		CLEI Code
Page00 193(C1h)	0x00	0		CLEI Code
Page00 194(C2h)	0x00	0		CLEI Code
Page00 195(C3h)	0x00	0		CLEI Code
Page00 196(C4h)	0x00	0		CLEI Code
Page00 197(C5h)	0x00	0		CLEI Code
Page00 198(C6h)	0x00	0		CLEI Code
Page00 199(C7h)	0x00	0		CLEI Code
Page00 200(C8h)	0xE0	224	?	Module Power Characteristics
Page00 201(C9h)	0x78	120	x	Module Power Characteristics
Page00 202(CAh)	0x00	0		Cable assembly length
Page00 203(CBh)	0x00	0		Media Connector Type
Page00 204(CCh)	0x00	0		Copper Cable Attenuation
Page00 205(CDh)	0x00	0		Copper Cable Attenuation
Page00 206(CEh)	0x00	0		Copper Cable Attenuation
Page00 207(CFh)	0x00	0		Copper Cable Attenuation
Page00 208(D0h)	0x00	0		Copper Cable Attenuation
Page00 209(D1h)	0x00	0		Copper Cable Attenuation
Page00 210(D2h)	0x00	0		Cable Assembly Lane Information
Page00 211(D3h)	0x00	0		Cable Assembly Lane Information
Page00 212(D4h)	0x00	0		Media Interface Technology
Page00 213-220 (D5h-DCh)	0x00	0		Reserved
Page00 221(DDh)	0x00	0		Custom
Page00 222(DEh)	0x00	0		Checksum

Page00 223-255 (DFh-FFh)	0x00	0		Custom Info NV
Page01 128(80h)	0x00	0		Inactive Major FW Rev
Page01 129(81h)	0x00	0		Inactive Minor FW Rev
Page01 130(82h)	0x01	1		Module Major HW Rev
Page01 131(83h)	0x01	1		Module Minor HW Rev
Page01 132(84h)	0x00	0		link length SMF
Page01 133(85h)	0x00	0		link length (OM5)
Page01 134(86h)	0x00	0		link length (OM4)
Page01 135(87h)	0x00	0		link length (OM3)
Page01 136(88h)	0x00	0		link length (OM2)
Page01 137(89h)	0x00	0		Reserved
Page01 138(8Ah)	0x00	0		Nominal Wavelength
Page01 139(8Bh)	0x00	0		Nominal Wavelength
Page01 140(8Ch)	0x00	0		Wavelength Tolerance
Page01 141(8Dh)	0x00	0		Wavelength Tolerance
Page01 142(8Eh)	0x04	4		Implemented Management Interface features advertising
Page01 143(8Fh)	0xDF	223	?	Implemented Management Interface features advertising
Page01 144(90h)	0x00	0		Implemented Management Interface features advertising
Page01 145(91h)	0x04	4		Module Characteristics advertising
Page01 146(92h)	0x55	85	U	Module Characteristics advertising
Page01 147(93h)	0xD8	216	?	Module Characteristics advertising
Page01 148(94h)	0x00	0		Module Characteristics advertising
Page01 149(95h)	0x00	0		Module Characteristics advertising
Page01 150(96h)	0x91	145	?	Module Characteristics advertising
Page01 151(97h)	0x00	0		Module Characteristics advertising
Page01 152(98h)	0x00	0		Module Characteristics advertising
Page01 153(99h)	0x00	0		Module Characteristics advertising
Page01 154(9Ah)	0x00	0		Module Characteristics advertising
Page01 155(9Bh)	0x00	0		Implemented Controls advertising
Page01 156(9Ch)	0x00	0		Implemented Controls advertising

Page01 157(9Dh)	0x00	0		Implemented Flags advertising
Page01 158(9Eh)	0x00	0		Implemented Flags advertising
Page01 159(9Fh)	0x23	35	#	Implemented Monitors advertising
Page01 160(A0h)	0x00	0		Implemented Monitors advertising
Page01 161(A1h)	0x08	8		Implemented Signal Integrity Controls advertising
Page01 162(A2h)	0x00	0		Implemented Signal Integrity Controls advertising
Page01 163-166 (A3h-A6h)	0x00	0		
Page01 167(A7h)				State Machine Duration advertising
Page01 168-175(A8h-AFh)	0x00	0		
Page01 176(B0h)	0x01	1		Media side lane assignment advertising for AppSel code 1
Page01 177(B1h)	0x01	1		Media side lane assignment advertising for AppSel code 2
Page01 178-254(B2h-FEh)				
Page01 255(FFh)				Checksum
Page02 128(80h)	0x50	80		Temperature monitor high alarm threshold MSB
Page02 129(81h)	0x00	0		Temperature monitor high alarm threshold LSB
Page02 130(82h)	0x00	0		Temperature monitor low alarm threshold MSB
Page02 131(83h)	0x00	0		Temperature monitor low alarm threshold LSB
Page02 132(84h)	0x4B	75		Temperature monitor high warning threshold MSB
Page02 133(85h)	0x00	0		Temperature monitor high warning threshold LSB
Page02 134(86h)	0x05	5		Temperature monitor low warning threshold MSB
Page02 135(87h)	0x00	0		Temperature monitor low warning threshold LSB
Page02 136(88h)	0x8C	140	?	Supply 3.3-volt monitor high alarm threshold MSB
Page02 137(89h)	0xA0	160	?	Supply 3.3-volt monitor high alarm threshold LSB
Page02 138(8Ah)	0x75	117	u	Supply 3.3-volt monitor low alarm threshold MSB
Page02 139(8Bh)	0x30	48	0	Supply 3.3-volt monitor low alarm threshold LSB
Page02 140(8Ch)	0x8A	138	?	Supply 3.3-volt monitor high warning threshold MSB
Page02 141(8Dh)	0xAC	172	?	Supply 3.3-volt monitor high warning threshold LSB
Page02 142(8Eh)	0x77	119	w	Supply 3.3-volt monitor low warning threshold MSB
Page02 143(8Fh)	0x24	36	$	Supply 3.3-volt monitor low warning threshold LSB

Page02 144-254 (90h-FEh)	0x00	0		
Page02 255(FFh)	0x00	0		Checksum
Page03 128-131(80h-83h)	0x00	0		User EEPROM
Page03 132(84h)	0x00	0		Insertion Counter MSB
Page03 133(85h)	0x00	0		Insertion Counter LSB
Page03 134(86h)	0x55	85	d	Cut-Off temperature
Page03 135(87h)	0x00	0		Power control registers
Page03 136(88h)	0x00	0		Power control registers
Page03 137(89h)	0x00	0		Power control registers
Page03 138(8Ah)				
Page03 139(8Bh)	0x00	0		Digital Status of the low speed signals.
Page03 140(8Ch)	0x00	0		IntL Control Register
Page03 141(8Dh)	0x13	19		BER period MSB
Page03 142(8Eh)	0x88	136		BER period LSB
Page03 143(8Fh)				Internally measured Temperature T.S.2 MSB
Page03 144(90h)				Internally measured Temperature T.S.2 LSB
Page03 145-169(8Fh-A9h)				Reseved
Page03 170-171(AAh-ABh)	0x00	0		User EEPROM
Page03 172(ACh)				TXin lane 1 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 173(ADh)				TXin lane 2 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 174(AEh)				TXin lane 3 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 175(AFh)				TXin lane 4 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 176(B0h)				TXin lane 5 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 177(B1h)				TXin lane 6 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 178(B2h)				TXin lane 7 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 179(B3h)				TXin lane 8 equalizer VGA digital gain Range from 0 to 31 (0 : no gain , 31 : highest gain)
Page03 180-255(B4h-FFh)	0x00	0		User EEPROM

2.2.4 Memory Accessibility

The Memory Map registers types are shown in the table below:

Page Address	Address Range	Type
Lower Page	0-25	RO
	26	RW (VR)
	27-126	RO
	127	RW (VR)
Page 00h	128-165	RO
	166-181	RW (NVR)
	182-255	RO
Page 01h	128-255	RO
Page 02h	128-255	RO
Page 03	128-129	RW (NVR)
	130	RO
	131	RW (NVR)
	132-133	RO
	134-138	RW (NVR)
	139	RO
	140	RW (NVR)
	141-142	RW (NVR)
	143-169	RO
	170-155	RW (NVR)
Page 16	128-255	RW (VR)
Page 19	128-143	RO
	144-176	RW (VR)
	176	RO
	177	RW (VR)
	178	RO
	179-255	RW VR
Page 20	128	RW (NVR)
	129-255	RO (VR)
Page B0	128-255	RW (NVR)
Page B1	128-255	RW (NVR)
Page B2	128-255	RW (NVR)
Page B3	128-255	RW (NVR)
Page B4	128-255	RW (NVR)
Page B5	128-255	RW (NVR)
Page B6	128-255	RW (NVR)
Page B7	128-255	RW (NVR)
Page B8	128-255	RW (NVR)
	129	RW (VR)

2.3 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- INT/RSTn
- LPW/PRSn

2.3.1 INT/RSTn

INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.
Reset is an active low signal on the host which is translated to an active low signal on the module.
Interrupt is an active high signal on the module which gets translated to an active low signal on the host.

2.3.2 LPWn/PRSn

LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present.
Low Power mode is an active low signal on the host which gets converted to an active low signal on the module.
Module Present is controlled by a pull down resistor on the module which gets converted to an active low logic signal on the host.

2.4 ML4064-ALB2-112 Specific Functions

2.4.1 Module State

The Module State describes module-wide behaviors and properties. The **ML4064-ALB2-112** implements two module states: ModuleLowPwr and ModuleReady.

The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the Module is in Low Power mode, where the Power Spots are deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.
The ModuleReady state is a host control state that indicates that the module is in High Power mode, and the PWM is activated. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
3 (lower Page)	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

2.4.2 Module State Transition

The state transition between Module Low Power and Module Ready is related to three parameters:

1. LowPwrRequestSW bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwrAllowRequestHW bit – software control, register 26 bit 6
3. LPWn – Hardware signal

According to these parameters, the state of the module is defined. Conditions for low-power state and ready state are summarized in the table below.

LowPwrRequestSW (Reg 26 bit 4)	LowPwrAllowRequestHW (register 26 bit 6)	LPWn	State
1	X	X	Module Low Pwr
0	1	0	Module Low Pwr
0	1	1	Module Ready
0	0	0	Module Ready
0	0	1	Module Ready

2.4.3 Module Global Controls

Module global controls are control aspects that are applicable to the entire module or all channels in the module.

Address	Bit	Name	Description	Type
26 (lower Page)	6	LowPwrAllowRequestHW	Parameter used to control the module power mode (refer to section 2.4.2) Default value =1	RW
	4	LowPwrRequestSW	0b = high power mode(default) 1b =Forces module into low power mode	
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for the appropriate hold time, followed by its de-assertion. This bit is self-clearing. 0b = not in reset 1b = Software reset	
3 (lower page)	0	Software Interrupt	Digital state of Interrupt: 0b = Interrupt source is present 1b = No interrupt source present	RO

2.4.4 Temperature Monitor

The **ML4064-ALB2-112** has 2 internal temperature sensors on the PCBA to continuously monitor the module temperature. In addition to one temperature monitor for the transceiver chip. Internally measured Module temperatures are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –127°C to +128°C that is considered valid between –40° and +125° C.

Address	Bit	Name	Description	Type
14 Lower Page	All	Temperature MSB	Internally measured TempSense2 (PCB Top)	RO
15 Lower Page	All	Temperature LSB		
143 Page 03h	All	Temperature MSB	Internally measured TempSense1 (PCB Top)	
144 Page 03h	All	Temperature LSB		
24 Lower Page	All	Temperature MSB	Internally measured transceiver temperature	
25 Lower Page	All	Temperature LSB		

The distribution of internal temperature sensors is shown in the figure below.

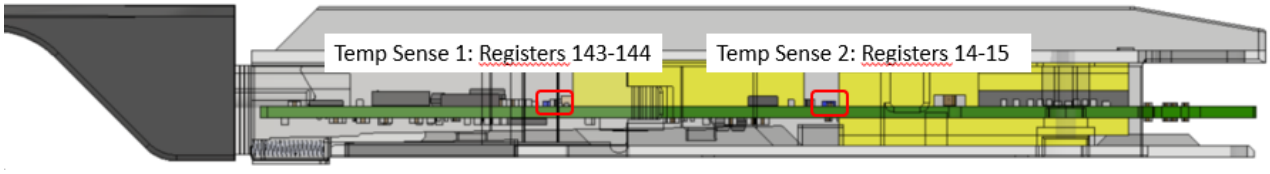

Figure 5: Temperature sensors location

The temperature alarms and warnings interrupt flags exist in lower page.

Address	Bit	Name	Description	Type
9 (lower Page)	3	L-Temp Low Warning	Latched low temperature warning flag	RO
	2	L-Temp High Warning	Latched high temperature warning flag	
	1	L-Temp Low Alarm	Latched low temperature alarm flag	
	0	L-Temp High Alarm	Latched high temperature alarm flag	

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0.

2.4.5 Voltage Sense

A voltage sense circuit is available in the **ML4064-ALB2-112** that allows to measure the internal module supplied voltage VCC, with LSB unit is 0.1 mV.

Address	Bit	Name	Description	Type
16	All	Supply voltage MSB	Internally measured supply voltage	RO
17	All	Supply voltage LSB	Internally measured supply voltage	

The Voltage alarms and warnings interrupt flags exists in lower page.

Address	Bit	Name	Description	Type
9 (lower Page)	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	RO
	6	L-Vcc3.3v High Warning	Latched low 3.3 volts supply voltage warning flag	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	4	L-Vcc3.3v High Alarm	Latched low 3.3 volts supply voltage alarm flag	

2.4.6 Programmable Power Dissipation and Thermal Emulation

The power spots are distributed on a separate board, a daughter card that is mounted on the PCBA, which contains only the power spots.
The daughter card contains three thermal spots that are heated relative to the related control registers settings. The distribution of these spots is shown in the image below (Figure6).

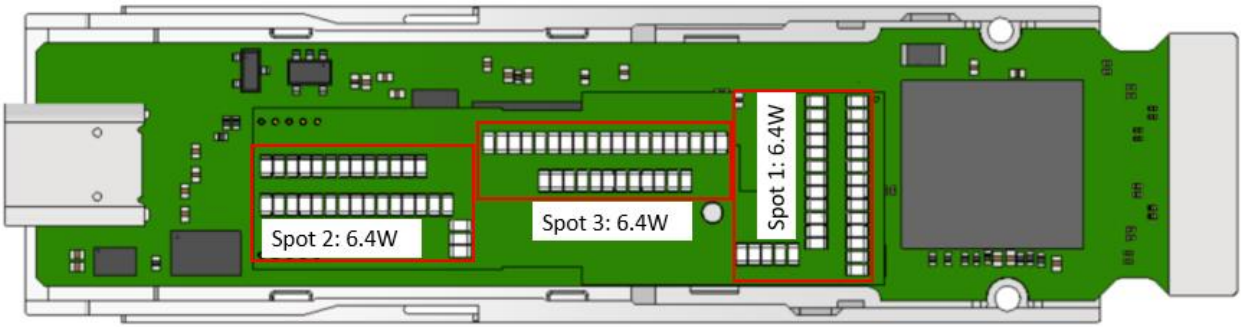

Figure 6: Thermal spots distribution

Registers 135, 136 and 137, page 03h are used to control thermal spots over I2C. They are 8-bits data wide registers.
The consumed power changes accordingly when the values of these registers are changed (only in high power mode). In Low-power mode the module automatically turns off all power spots. The values written in these registers are permanently stored.

The control registers of the thermal spots are shown in the table below:

Address	Bit	Name	Description	Memory Type
135	7:0	PWM Controller 1	6.4W power spot PWM Control Register (P3V3_Spots)	RW (NVR)
136	7:0	PWM Controller 2	6.4 W power spot PWM Control Register (P3V3_Spots)	
137	7:0	PWM Controller 3	6.4 W power spot PWM Control Register (P3V3_Spots)	

The Figure 7 shows a side view of the distribution of Thermal Interface used to allow the heat conduction from the PCB to the shell.

Figure 7: Thermal Interfaces Distribution

2.4.7 Maximum Power Indicator

The maximum power in the module is indicated by reading register 201 of Page 00.

Address	Page	Bit	Name	Description	Default	Type
201	Page 00	All	Max Power Indicator	**Module Maximum Power Consumption**	Decimal : 120 Corresponding to 30W	RO

2.4.8 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, all power spots will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, the PWM goes back to its previous value.
The **ML4064-ALB2-112** is set to its maximum Cut-Off temperature of 85˚C by default, and can be programmed to any value from register 134 of memory page 03.

Address	Bit	Name	Description	Type
134	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW (NVR)

2.4.9 Insertion counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 132-133 page 03.

Address	Bit	Name	Description	Type
132 (page 03)	MSB	Insertion Counter MSB		RO
133 (page 03)	LSB	Insertion Counter LSB	LSB unit = 1 insertion	

2.4.10 Alarm and warning thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory-preset values allow you to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page 02.

Address	Bit	Name	Default Value	Type
128(page 02)	ALL	high temp alarm threshold (MSB)	80˚C	RO
129(page 02)	ALL	high temp alarm threshold (LSB)		
130(page 02)	ALL	low temp alarm threshold (MSB)	0° C	
131(page 02)	ALL	low temp alarm threshold (LSB)		
132(page 02)	ALL	high temp warning threshold (MSB)	75˚C	
133(page 02)	ALL	high temp warning threshold (LSB)		
134(page 02)	ALL	low temp warning threshold (MSB)	5˚C	
135(page 02)	ALL	low temp warning threshold (LSB)		
136(page 02)	ALL	high volt alarm threshold (MSB)	3.6 V	

137(page 02)	ALL	high volt alarm threshold (LSB)		
138(page 02)	ALL	low volt alarm threshold (MSB)	3.0 V	
139(page 02)	ALL	low volt alarm threshold (LSB)		
140(page 02)	ALL	high volt warning threshold (MSB)	3.55 V	
141(page 02)	ALL	high volt warning threshold (LSB)		
142(page 02)	ALL	low volt warning threshold (MSB)	3.05 V	
143(page 02)	ALL	low volt warning threshold (LSB)		

2.4.11 Low Speed Signals Pin Status

The register below is accessed from page 03h.

Address	Page	Bit	Name	Description	Type
139	Page 03	5	LPWn signal State Transition	Read 0b: No edge detected Read 1b: Either rising edge or falling edge crossing the 1.25V threshold is detected Write 0b: No effect Write 1b: Clear the register	RO
		1	LPWn logic status	Read 1b: High Read 0b: Low	RW

2.4.12 INTL Control

During power-up of the module, INT is defaulted to negated. Afterward, host can set the status of this indicator to any status through an I2C registers **in upper page 03**. Setting it should not affect any operation in the module.

Address	Page	Bit	Name	Description	Type
140	Page 03	1:0	IntL Control	Digital Control of INTL: 0x: Normal Operation 10: Force M_INT to logic 0 11: Force the M_INT to logic 1	RW

In “Normal Operation”, the INTL is asserted when the alarm is high (VCC or Temperature).

3 High Speed

The **ML4064-ALB2-112** includes a low power 800G retimer transceiver chip. The transceiver operates at 53.125 PAM4, Gray coded pattern. The default mode of operation is the retimed loopback mode.

3.1 Advertisement

This paragraph lists the module supported features and capabilities. All registers mentioned in the table below are present in page 13h.

Address	Bit	Name	Description	Default Value	Type
128	4	PerLaneHostSideLoopbacks	0b: Not supported 1b: Supported	0	RO
	3	HostSideInputLoopback	0b: Not supported 1b: Supported	1	
129	7-6	GatingSupport	0: Not Supported 1: Supported with time accuracy <= 2 ms 2: Supported with time accuracy <= 20 ms 3: Supported with time accuracy > 20 ms	0	RO
	5	GatingResultsSupported	Gating result statistics selectable by diagnosticsSelector (14h:128) values 11h-15h are: 0b: Not supported 1b: Supported	0	
	4	PeriodicUpdatesSupported	Realtime statistics selectable by DiagnosticsSelector (14h:128) values 01h-06h are periodically updated during measurement: 0b: no periodic update during measurement 1b: periodic update during measurement	1	
	3	PerLaneGatingTimersSupported	0b: Only two global gating timers are available for all lanes on all Banks, one for Host Side Measurements and one for Media Side Measurements. 1: Per lane gating timers are supported in all Banks	0	
	2	AutoRestartGatingSupported	0b: AutoRestartGating control (13h:177.4) not supported 1b: AutoRestartGating control (13h:177.4) supported	0	
130	4	HostSideInputSNRMeasurement	Indicates if hos side SNR measurement reported via Diagnostics Selection value 06h is supported (Byte 14h:128) 1b: Supported 0b: Not supported	1	RO
	1	BitsAndErrorsCountingSupported	Indicates if DiagnosticsSelector values 02h-05h are supported (Page 14h byte 128, Table 8-114) 0b: Not supported 1b: Supported	1	
131	2	PRBSGeneratorHostSidePostFEC	0b: Not supported 1b: Supported	1	RO

	1	PRBSCheckerHostSidePreFEC	0b: Not supported 1b: Supported	1	
132	7	HostSideGeneratorSupportsPattern7	PRBS-13 (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	0	RO
	6	HostSideGeneratorSupportsPattern6	PRBS-13Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	1	
	5	HostSideGeneratorSupportsPattern5	PRBS-15 (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	0	
	4	HostSideGeneratorSupportsPattern4	PRBS-15Q (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	1	
	3	HostSideGeneratorSupportsPattern3	PRBS-23 (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	0	
	2	HostSideGeneratorSupportsPattern2	PRBS-23Q (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	1	
	1	HostSideGeneratorSupportsPattern1	PRBS-31 (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsPattern0	PRBS-31Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	1	
133	7	HostSideGeneratorSupportsPattern15	User Pattern (Programmable pattern provided in Bytes 13h:224-255): 0b: Not supported 1b: Supported	1	RO
	6	HostSideGeneratorSupportsPattern14	Custom Vendor defined pattern	1	
	5	HostSideGeneratorSupportsPattern13	Reserved	0	
	4	HostSideGeneratorSupportsPattern12	SSPRQ (As defined in IEEE 802.3-2018 clause 120.5.11.2.3)	1	
	3	HostSideGeneratorSupportsPattern11	PRBS-7 (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	0	
	2	HostSideGeneratorSupportsPattern10	PRBS-7Q (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	1	
	1	HostSideGeneratorSupportsPattern9	PRBS-9 (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsPattern8	PRBS-9Q (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported	1	

			1b: Supported		
136	7	HostSideCheckerSupportsPattern7	PRBS-13 (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	0	RO
	6	HostSideCheckerSupportsPattern6	PRBS-13Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.1): 0b: Not supported 1b: Supported	1	
	5	HostSideCheckerSupportsPattern5	PRBS-15 (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	0	
	4	HostSideCheckerSupportsPattern4	PRBS-15Q (x^15 + x^14 + 1): 0b: Not supported 1b: Supported	1	
	3	HostSideCheckerSupportsPattern3	PRBS-23 (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	0	
	2	HostSideCheckerSupportsPattern2	PRBS-23Q (ITU-T Recommendation O.172, 2005): 0b: Not supported 1b: Supported	1	
	1	HostSideCheckerSupportsPattern1	PRBS-31 (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	0	
	0	HostSideCheckerSupportsPattern0	PRBS-31Q (As defined in IEEE 802.3-2018 clause 120.5.11.2.2): 0b: Not supported 1b: Supported	1	
137	7	HostSideCheckerSupportsPattern15	User Pattern (Programmable pattern provided in Bytes 13h:224-255): 0b: Not supported 1b: Supported	0	RO
	6	HostSideCheckerSupportsPattern14	Custom Vendor defined pattern	0	
	5	HostSideCheckerSupportsPattern13	Reserved	0	
	4	HostSideCheckerSupportsPattern12	SSPRQ (As defined in IEEE 802.3-2018 clause 120.5.11.2.3)	0	
	3	HostSideCheckerSupportsPattern11	PRBS-7 (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	0	
	2	HostSideCheckerSupportsPattern10	PRBS-7Q (x^7 + x^6 + 1): 0b: Not supported 1b: Supported	1	
	1	HostSideCheckerSupportsPattern9	PRBS-9 (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	0	
	0	HostSideCheckerSupportsPattern8	PRBS-9Q (As defined in IEEE 802.3-2018 clause 120.5.11): 0b: Not supported 1b: Supported	1	

140	7-6	RecoveredClockForGeneratorOptions	Options to use recovered clock for contra-directional pattern generator on the same module side: 00b: not supported 01b: supported without loopback 10b: supported with loopback 11b: supported with and without loopback	0b10	RO
	5	ReferenceClockForPatternsSupported	option to use reference clock for pattern generation: 0b: Not supported 1b: Supported	1	
	3-0	UserPatternLengthSupported	Maximum length L of the user defined pattern, where the field value n encodes L as L=2(n+1), i.e. 0000b: 2 bytes, …, 1111b: 32 bytes	0b0111	
141	3	HostSideCheckerSupportsDataSwap	Register 162 for swapping the MSB and LSB for PAM4 patterns: 0b: Not supported 1b: Supported	0	RO
	2	HostSideCheckerSupportsDataInvert	Register 161 for pattern inversion: 0b: Not supported 1b: Supported	0	
	1	HostSideGeneratorSupportsDataSwap	Register 146 for swapping the MSB and LSB for PAM4 patterns: 0b: Not supported 1b: Supported	0	
	0	HostSideGeneratorSupportsDataInvert	Register 145 for pattern inversion: 0b: Not supported 1b: Supported	0	
142	3	HostCheckerSupportsPerLaneEnable	Host Side pattern checker for lane i enabled in 13h:160 enables lane i 0b: per lane enable not supported 1b: per lane enable supported	1	RO
	2	HostCheckerSupportsPerLanePattern	Host Side pattern selection for checker 0b: Lane 1 Pattern Type 13h:164.3-0 is used for all lanes. 1b: Per lane Pattern selection 13h:164-167	1	
	1	HostGeneratorSupportsPerLaneEnable	Host Side pattern generator for lane i enabled in 13h:144 enables lane i 0b: per lane enable not supported 1b: per lane enable supported	1	
	0	HostGeneratorSupportsPerLanePattern	Host Side pattern selection for generator 0b: Lane 1 Pattern 13h:148.3-0 is used for all lanes. 1b: Per lane Pattern selection 13h.148-151	1	

3.2 PRBS Generator

The Pattern Generator control is described in this section. The generated pattern is transmitted from the module to the host on the RX electrical output. The PRBS generator control registers are present in Page 13h. the PRBS generator mode is enabled automatically when the Loopback mode is disabled.

Address	Bit	Name	Description	Default Value	Type
144	7	HostSideGeneratorEnableLane8	0b: Disable pattern generator 1b: Enable pattern generator	0	RW (VR)
	6	HostSideGeneratorEnableLane7		0	
	5	HostSideGeneratorEnableLane6		0	
	4	HostSideGeneratorEnableLane5		0	
	3	HostSideGeneratorEnableLane4		0	
	2	HostSideGeneratorEnableLane3		0	
	1	HostSideGeneratorEnableLane2		0	
	0	HostSideGeneratorEnableLane1		0	
148	7-4	HostSideGeneratorPatternSelectLane2	The Pattern IDs are summarized below: 0: PRBS-31Q 1: PRBS-31 2: PRBS-23Q 3: PRBS-23 4: PRBS-15Q 5: PRBS-15 6: PRBS-13Q 7: PRBS-13 8: PRBS-9Q 9: PRBS-9 10: PRBS-7Q 11: PRBS-7 12: SSPRQ 13: Reserved 14: Custom 15: User Pattern	0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane1		0x0	
149	7-4	HostSideGeneratorPatternSelectLane4		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane3		0x0	
150	7-4	HostSideGeneratorPatternSelectLane6		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane5		0x0	
151	7-4	HostSideGeneratorPatternSelectLane8		0x0	RW (VR)
	3-0	HostSideGeneratorPatternSelectLane7		0x0	
176	7-4	HostPRBSGeneratorClockSource	0: All lanes uses Internal Clock 1: All lanes uses Recovered Clock Media Lane 1 2: All lanes uses Recovered Clock Media Lane 2 3: All lanes uses Recovered Clock Media Lane 3 4: All lanes uses Recovered Clock Media Lane 4 5: All lanes uses Recovered Clock Media Lane 5 6: All lanes uses Recovered Clock Media Lane 6 7: All lanes uses Recovered Clock Media Lane 7 8: All lanes uses Recovered Clock Media Lane 8 Ah-Eh: Reserved Fh: Recovered clock from Respective Media Lane/Datapaths are used	0b0000	RO (VR)
224-239	7-0	UserPattern	Host defined user pattern (16 Bytes)	-First 8 bytes: 0xFF -Last 8 bytes: 0x00	RW (VR)

3.3 PRBS Checker

The pattern Checker control is described in this section. The control is applied on the host side of the module for data received at the TX electrical input. The PRBS checker control registers are present in Page 13h. the PRBS checker mode is enabled by default.

The PRBS checker behavior described in this section is for the un-gated mode (13h:177.3-1 = 000b). In this mode, the error metrics measurement runs continuously. When the host enables the disabled PRBS checkers (register 160 in the table below) all error counters for the enabled lanes are cleared and then start accumulating. When the host disables enabled PRBS checkers (register 160 in the table below) error counting is stopped, and error counting results will be available via Selector 01-05h.
The error information availability is related to the PeriodicUpdatesSupported settings (13h:129.4):

- 13h:129.4 = 0: real time error information is not updated and error information is only available when the error counting is stopped by checker disable
- 13h:129.4 = 1: real time error information is available with Selectors 01-05h. Update period is configured by 13h:177.0, as described in section 3.5.1.

The error counters and restart accumulation are controlled form ResetErrorInformation control bit 13h:177.5, as described in section 3.5.1.

Address	Bit	Name	Description	Default Value	Type
160	7	HostSideCheckerEnableLane8	0b: Disable pattern Checker 1b: Enable pattern Checker	1	RW (VR)
	6	HostSideCheckerEnableLane7		1	
	5	HostSideCheckerEnableLan6		1	
	4	HostSideCheckerEnableLane5		1	
	3	HostSideCheckerEnableLane4		1	
	2	HostSideCheckerEnableLane3		1	
	1	HostSideCheckerEnableLane2		1	
	0	HostSideCheckerEnableLane1		1	
164	7-4	HostSideCheckerPatternSelectLane2	The Pattern IDs are summarized below: 0: PRBS-31Q 1: PRBS-31 2: PRBS-23Q 3: PRBS-23 4: PRBS-15Q 5: PRBS-15 6: PRBS-13Q	0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane1		0x0	
165	7-4	HostSideCheckerPatternSelectLane4		0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane3		0x0	

166	7-4	HostSideCheckerPatternSelectLane6	7: PRBS-13 8: PRBS-9Q 9: PRBS-9 10: PRBS-7Q 11: PRBS-7 12: SSPRQ 13: Reserved 14: Custom 15: User Pattern	0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane5		0x0	
167	7-4	HostSideCheckerPatternSelectLane8		0x0	RW (VR)
	3-0	HostSideCheckerPatternSelectLane7		0x0	
178	3-2	HostPRBSCheckerClockSource	0: Recovered clocks from Respective Host Lane/Datapaths are used 1: All lanes use Internal Clock 2: All lanes use reference clock 3: reserved	0b01	RO (VR)

3.3.1 PRBS Checker Lock Status

In PRBS Checker mode, the loss of lock (LOL) status is reported in register 138 of Page 14h.

Address	size	Name	Description	Default Value	Type
138	7	PatternCheckerLOLFlagHostLane8	-0b: no LOL is detected (Locked) -1b: LOL is detected (not Locked)	0	RO
	6	PatternCheckerLOLFlagHostLane7		0	
	5	PatternCheckerLOLFlagHostLane6		0	
	4	PatternCheckerLOLFlagHostLane5		0	
	3	PatternCheckerLOLFlagHostLane4		0	
	2	PatternCheckerLOLFlagHostLane3		0	
	1	PatternCheckerLOLFlagHostLane2		0	
	0	PatternCheckerLOLFlagHostLane1		0	

3.4 Loopback

The Host side loopback control registers are described in the table below. These registers are present in Page 13h. The Loopback mode is the default mode of the module. Writing 0x00 to register 183 will enable the PRBS Generator mode.

Address	size	Name	Description	Default Value	Type
183	7	HostSideInputLoopbackEnableLane8	-0b: PRBS Generator / Checker mode -1b: Retimed Loopback Mode Writing 1 to any of the register 183 bits will enable the Loopback mode on all channels.	1	RW (VR)
	6	HostSideInputLoopbackEnableLane7		1	
	5	HostSideInputLoopbackEnableLane6		1	
	4	HostSideInputLoopbackEnableLane5		1	
	3	HostSideInputLoopbackEnableLane4		1	
	2	HostSideInputLoopbackEnableLane3		1	
	1	HostSideInputLoopbackEnableLane2		1	

	0	HostSideInputLoopbackEnableLane1		1	

3.5 BER/SNR

The BER and SNR data and control are described in this section.

3.5.1 Error Information Reset and Update Period

The error information reset and update period control register 177 is present in Page 13h.

Address	Bit	Name	Description	Default Value	Type
177	5	ResetErrorInformation	This bit is used to clear the error counters and restart accumulation of errors. -13h:177.5 = 1b: Currently accumulating error statistics identified by DiagnosticsSelector 01h to 05h are frozen -13h:177.5 = 0b: Error statistics identified by Selectors 01h-05h are reset to 0 When configuration in 13h:129.3=0b there is only 1 timer for all lane and all banks. Setting this bit to 1b: single gate timer is stopped Setting this bit to 0b: starts the single gating timer	0	RW (VR)
	0	UpdatePeriodSelect	Time between incremental updates to intermediate error counting results during a longer gating period 0b: 1 sec update interval 1b: 5 sec update interval	1	RW (NVR)

3.5.2 Diagnostics Selector

The diagnostics selector is described in the table below. It is controlled from register 128 of Page 14h. This register controls the content of diagnostics data registers.

Address	Bit	Name	Description	Default Value	Type
128	7-0	DiagnosticsSelector	Select content of Diagnostics Data in bytes 192-255: -0x02: Host Lane 1-4 errors and total Bits counters (gives the host the ability to read the running BER while gating is in progress) -0x03: Host Lane 5-8 errors and total Bits counters (gives the host the ability to read the running BER while gating is in progress) -0x06: Host/Media Input Lane 1-8 SNR	0	RW (VR)

3.5.3 BER Diagnostics

The tables below show the registers reporting the errors count and the total bit counters for each channel. The mentioned registers are present in Page 14h. The reported channels are related to the value set in register 128 of page 14h as detailed in section 3.5.2.

For detailed info on how error count is reported, refer to section 3.3.

In case of 14h:128 = 0x02, check the table below.

Address	size	Name	Description	Default Value	Type
192-199	8	HostSideErrorCountLane1	U64 Little-endian error count Lane 1	0	RO (VR)
200-207	8	HostTotalBitsCountLane1	U64 Little-endian total bit count 1	0	
208-215	8	HostSideErrorCountLane2	U64 Little-endian error count Lane 2	0	
216-223	8	HostTotalBitsCountLane2	U64 Little-endian total bit count 2	0	
224-231	8	HostSideErrorCountLane3	U64 Little-endian error count Lane 3	0	
232-239	8	HostTotalBitsCountLane3	U64 Little-endian total bit count 3	0	
240-247	8	HostSideErrorCountLane4	U64 Little-endian error count Lane 4	0	
248-255	8	HostTotalBitsCountLane4	U64 Little-endian total bit count 4	0	

In case of 14h:128 = 0x03, check the table below.

Address	size	Name	Description	Default Value	Type
192-199	8	HostSideErrorCountLane5	U64 Little-endian error count Lane 5	0	RO (VR)
200-207	8	HostTotalBitsCountLane5	U64 Little-endian total bit count 5	0	
208-215	8	HostSideErrorCountLane6	U64 Little-endian error count Lane 6	0	
216-223	8	HostTotalBitsCountLane6	U64 Little-endian total bit count 6	0	
224-231	8	HostSideErrorCountLane7	U64 Little-endian error count Lane 7	0	
232-239	8	HostTotalBitsCountLane7	U64 Little-endian total bit count 7	0	
240-247	8	HostSideErrorCountLane8	U64 Little-endian error count Lane 8	0	
248-255	8	HostTotalBitsCountLane8	U64 Little-endian total bit count 8	0	

3.5.4 SNR diagnostics

The table below shows the registers reporting the SNR for each channel at the host side. The mentioned registers are present in Page 14h. In this case 14h:128 should be set to 0x06, as described in section 3.5.2.

Address	size	Name	Description	Default Value	Type
208-209	2	HostSideSNRLane1	U16 Little-endian in units of 1/256dB host lane 1 real time SNR	0	RO

210-211	2	HostSideSNRLane2	U16 Little-endian in units of 1/256dB host lane 2 real time SNR	0	(VR)
212-213	2	HostSideSNRLane3	U16 Little-endian in units of 1/256dB host lane 3 real time SNR	0	
214-215	2	HostSideSNRLane4	U16 Little-endian in units of 1/256dB host lane 4 real time SNR	0	
216-217	2	HostSideSNRLane5	U16 Little-endian in units of 1/256dB host lane 5 real time SNR	0	
218-219	2	HostSideSNRLane6	U16 Little-endian in units of 1/256dB host lane 6 real time SNR	0	
220-221	2	HostSideSNRLane7	U16 Little-endian in units of 1/256dB host lane 7 real time SNR	0	
222-223	2	HostSideSNRLane8	U16 Little-endian in units of 1/256dB host lane 8 real time SNR	0	

3.6 TX and RX Control Fields

This section lists the specific controls for each TX and RX lane. The control registers mentioned in this section are present in Page 10h.

Address	size	Name	Description	Default Value	Type
129	7	InputPolarityFlipTx8	Input Polarity Flip control: -0b: No TX input polarity flip -1b: Tx input polarity flip	0	RW (VR)
	6	InputPolarityFlipTx7		0	
	5	InputPolarityFlipTx6		0	
	4	InputPolarityFlipTx5		0	
	3	InputPolarityFlipTx4		0	
	2	InputPolarityFlipTx3		0	
	1	InputPolarityFlipTx2		0	
	0	InputPolarityFlipTx1		0	
137	7	OutputPolarityFlipRx8	Output Polarity Flip control: -0b: No RX Output polarity flip -1b: RX Output polarity flip	0	RW (VR)
	6	OutputPolarityFlipRx7		0	
	5	OutputPolarityFlipRx6		0	
	4	OutputPolarityFlipRx5		0	
	3	OutputPolarityFlipRx4		0	
	2	OutputPolarityFlipRx3		0	
	1	OutputPolarityFlipRx2		0	
	0	OutputPolarityFlipRx1		0	
138	7	OutputDisableRx8	Output Disable control: -0b: RX Output enabled -1b: RX Output disabled	0	RW (VR)
	6	OutputDisableRx7		0	
	5	OutputDisableRx6		0	
	4	OutputDisableRx5		0	
	3	OutputDisableRx4		0	
	2	OutputDisableRx3		0	
	1	OutputDisableRx2		0	
	0	OutputDisableRx1		0	

3.7 Advanced Configuration

The high-speed interface configuration such as taps, gray mapping, signal type and baud rate can be controlled from PAGEB8. After any parameter is changed, apply configuration should be performed for the new settings take effect which can be done from register 130 of page B8h.

Address	bit	Name	Description	Default Value	Type
128	2	Taps control	0: 3-Taps FIR Mode 1: 7-Taps FIR Mode	1	RW (NVR)
	1	Gray mapping	0: Gray mapping disabled 1: Gray mapping enabled	1	
	0	Signal type	0: PAM signal type 1: NRZ signal type	0	
129	7-0	Baud Rate Select	0: 25.78125 GBaud 1: 26.5625 GBaud 2 : Reserved 3: 51.5625 GBaud 4: 53.125 GBaud 5 : 56.25 GBaud	0x04	
130	0	Apply Configuration	0 : do not apply 1 : Apply settings (self-clearing bit)	0	RW (VR)

3.8 Advanced Channel Configuration

RX output channels can be configured separately to tune the RX output signals. Each channel is controlled from a separate page, from B0h to B7h, for the register address range from 128 to 145.
The table below shows the page number corresponding to each channel.

Page Address	Description
B0	RXOUT 1 control page
B1	RXOUT 2 control page
B2	RXOUT 3 control page
B3	RXOUT 4 control page
B4	RXOUT 5 control page
B5	RXOUT 6 control page
B6	RXOUT 7 control page
B7	RXOUT 8 control page

After the page is the set, the corresponding parameters can be controlled, as described in the table below. Any change of the value in one of the following registers needs to apply configuration by writing 1 to register 130 Page B8h, as described in section 3.7.

The table below corresponds to Page B0h (RXOUT 1 control page).

Address	size	Name	Description	Default Value	Type
128	1	FIR Tap1 (MSB)	16-bit signed value: -1000 to +1000	0x00	RW (NVR)
129	1	FIR Tap1 (LSB)		0x0A	
130	1	FIR Tap2 (MSB)	16-bit signed value: -1000 to +1000	0xFF	
131	1	FIR Tap2 (LSB)		0xE4	
132	1	FIR Tap3 (MSB)	16-bit signed value: -1000 to +1000	0x00	
133	1	FIR Tap3 (LSB)		0x5A	
134	1	FIR Tap4 (MSB)	16-bit signed value: -1000 to +1000	0xFF	
135	1	FIR Tap4 (LSB)		0xEB	
136	1	FIR Tap5 (MSB)	16-bit signed value: -1000 to +1000	0x00	
137	1	FIR Tap5 (LSB)		0x07	
138	1	FIR Tap6 (MSB)	16-bit signed value: -1000 to +1000	0xFF	
139	1	FIR Tap6 (LSB)		0xFA	
140	1	FIR Tap7 (MSB)	16-bit signed value: -1000 to +1000	0xFF	
141	1	FIR Tap7 (LSB)		0xFD	
142	1	PAM4 Inner EYE (MSB)	16-bit signed value: -1000 to +1000	0x00	
143	1	PAM4 Inner EYE (LSB)		0x00	
144	1	PAM4 Outer EYE (MSB)	16-bit signed value: -1000 to +1000	0x00	
145	1	PAM4 Outer EYE (LSB)		0x00	

3.9 Advanced Channel Monitoring

Equalizer VGA gain can be monitored for TX input channels. VGA gain of all channels can be read from Page03 registers 172 to 179. The digital gain ranges between 0 for no gain and 31 for highest gain.

The VGA gain value is only valid when there is a PRBS checker lock on the TX input channel.

The table below shows the register addresses corresponding to each channel.

Register Address	Description
172(ACh)	TXin lane 1 equalizer VGA digital gain
173(ADh)	TXin lane 2 equalizer VGA digital gain
174(AEh)	TXin lane 3 equalizer VGA digital gain
175(AFh)	TXin lane 4 equalizer VGA digital gain
176(B0h)	TXin lane 5 equalizer VGA digital gain
177(B1h)	TXin lane 6 equalizer VGA digital gain
178(B2h)	TXin lane 7 equalizer VGA digital gain
179(B3h)	TXin lane 8 equalizer VGA digital gain

4 Module Connectivity

The **ML4064-ALB2-112** has a front USB-C connector allowing the user to access the following features:

- Reload registers
- FW upgrade

5 OSFP Pin Allocation

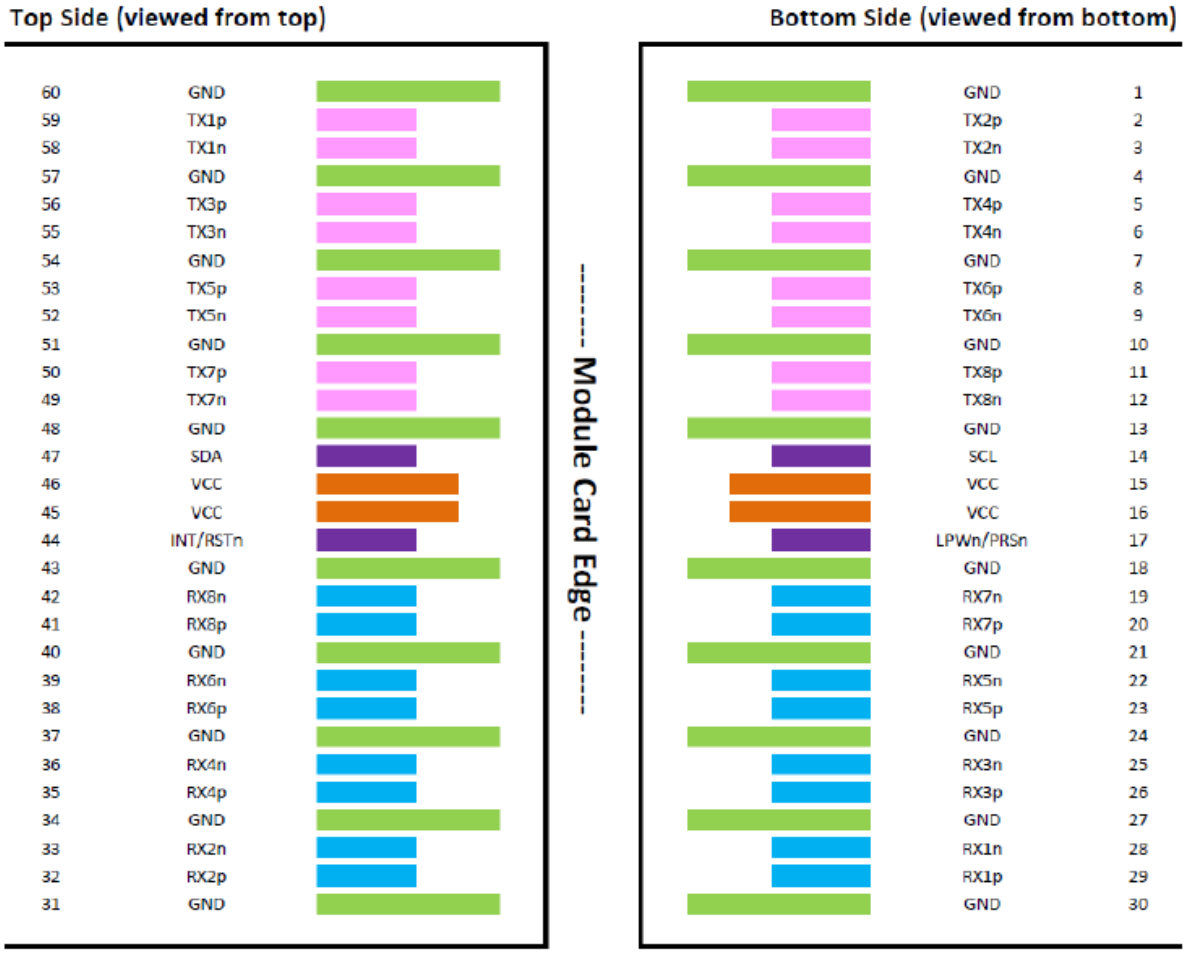

Figure 7: OSFP Module Pad Layout

6 Mechanical Dimensions – ML4064-ALB2-112

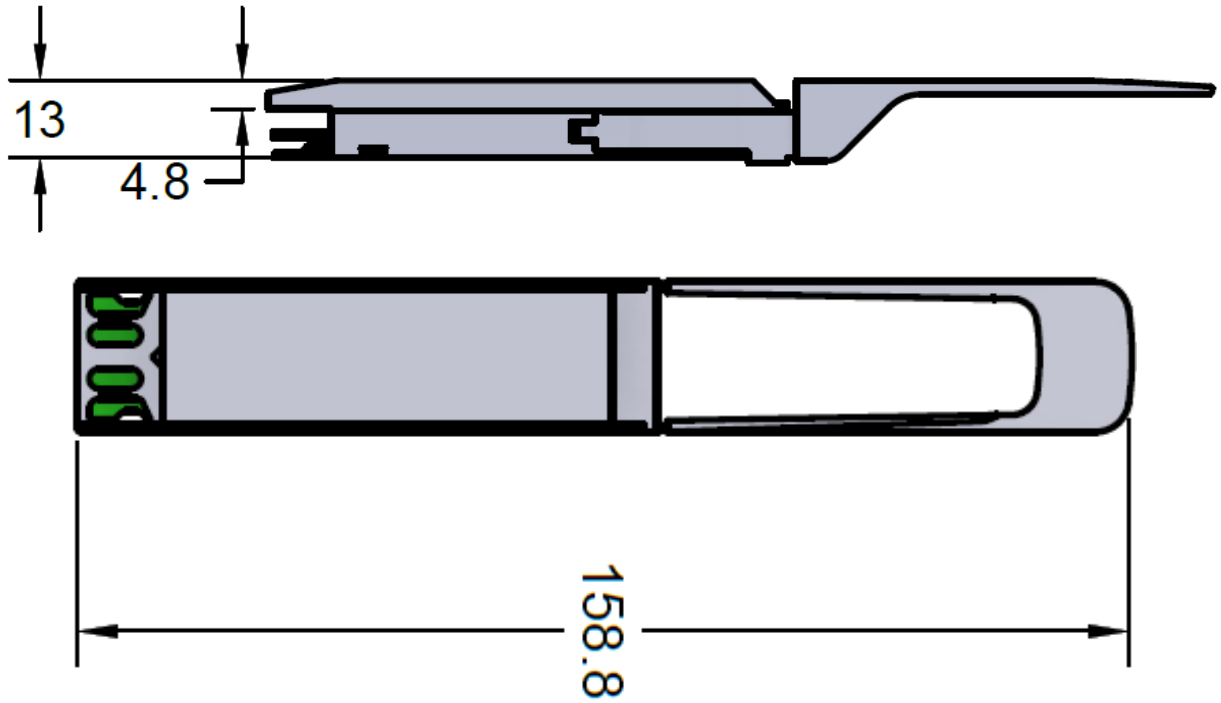

Figure 8: Mechanical Dimensions

7 Firmware Revision

FW Release	Upgrades
V1.0	▪ Initial FW release
V1.1	▪ Updated the content of some Application Descriptor registers ▪ Updated registers are located in lower memory page: registers 85 to 90 (content is shown in section 2.2.3)
V1.2	▪ Added AppSel code for 2×400G application in registers 90-94 of low memory page
V1.3	▪ TX input is set up for adaptive mode ▪ TX input EQ VGA gain can be read through registers 172-179 of page03. Range for each channel : 0 indicates no gain, and 31 indicates highest gain. ▪ State Machine Duration advertisement register 167 of page01 is updated to indicate timing between 10 and 50ms ▪ TX input support adaptive mode advertisement register 161 of page01 is updated to reflect adaptive mode ▪ AppSel code 2 memory location fixed in registers 90-93 of low memory page ▪ AppSel codes lane count for media interface is changed to 8 instead of 0 ▪ Media Side Lane Assignment for AppSel codes 1 and 2 are advertised in registers 176 and 177 of page01

Revision History

Revision number	Date	Description
0.1	8/10/2021	▪ Preliminary
0.2	7/4/2022	▪ Add cover image ▪ Update section 1 ▪ Remove section 1.3 ▪ Update section 2.2.3 ▪ Update section 2.2.4 ▪ Add section 2.4.1 ▪ Add section 2.4.2 ▪ Add section 2.4.3 ▪ Update section 2.4.4 ▪ Update section 2.4.6 ▪ Update section 2.4.7 ▪ Update section 2.4.11 ▪ Update section 2.4.12 ▪ Update section 6
0.3	7/6/2022	▪ Update PN ▪ Update section 2.2.3 ▪ Update section 2.2.4 ▪ Update section 2.4.4 ▪ Update section 2.4.6 ▪ Update section 3.7
0.4	7/8/2022	▪ Format fix
0.5	7/12/2022	▪ Update section 2.1.2: Management Timing Parameters ▪ Update section 2.4.4: fix mapping between registers and sensors ▪ Update section 3.2 and 3.3: default PRBS ▪ Update section 3.5.1 table for access type
0.6	8/4/2022	▪ Update section 2.2.3 : table content
0.7	8/16/2022	▪ Add section 7: Firmware Revision
0.8	11/3/2022	▪ Update section 2.2.3 ▪ Add section 3.9 ▪ Update section 7
0.9	12/8/2022	▪ Update section 3.8

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