multiLane

Marketing Datasheet

ML4070-SFP

Transceiver Margin Test Fixture

For SFP+/SFP28 Transceiver Testing Module Characterization

1-Lane 8.5-15 & 21-30 Gbps SFP28 Transceiver Test Set

VSR Trace Length Margining Power Supply Margining PS Noise Margining Bit Rate Margining Bathtub Curve Measurement Eye Contour Measurement Receiver Sensitivity



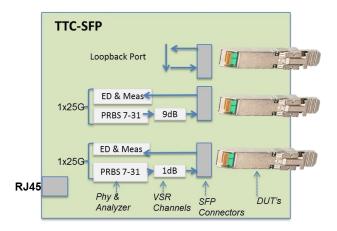
ML4070-SFP Marketing Datasheet

Advance Product information subject to change. Multilane SAL reserves the right to make changes to its product specifications at any time without notice. The information furnished herein is believed to be accurate; however, no responsibility is assumed for its use.



ML4070-SFP

SFP28 Transceiver Test Set



Summary

The ML4070-SFP is a state-of-the-art transceiver test set specifically designed for quick production testing of Go/No Go applications. It features Pulse Pattern Generators and Error Detectors as well as SFP host control circuitry with power supply noise injection capability. The ML4070 contains 3 SFP ports for 0 dB and 9 dB trace loss and for loopback.

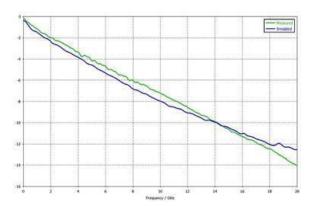
A full set of APIs and a production GUI enable quick one-button measurements and automatic report generation.

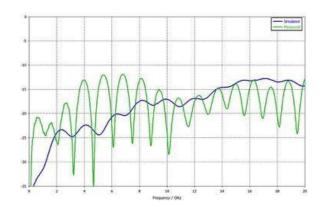
Key Features

- Operation 0 to 70°C
- DUT Voltage Margining 3.1 to 3.6V
- DUT Power Supply Noise Margin
- DUT Current Draw Measurement
- DUT State Machine Interface and MSA configuration
- BER graphs as a function of (PS voltage, PS noise, Bit Rate ±100ppm
- MSA Compatible QSFP MCB Eye Contour measurements

- Pre-emphasis tolerance Testing
- GUI and API control

S21 & S11 Characteristics of the 9dB Port





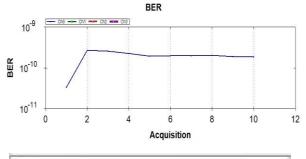
ML4070 BERT GUI

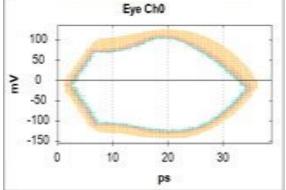
- BER test
- Support BER curve
- Provide multiple and single layouts of bathtub and eye contour

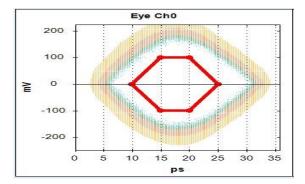
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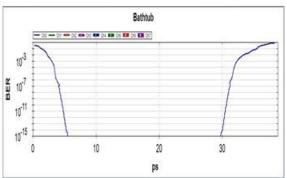
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Parameters	Specifications
Bit Rate	8.5-15 &21-30Gbps
Pattern	PRBS 7, 9, 15, 23, 31, and User Defined Pattern 16 bits@10G & 40 bits@25G
TX Amplitude Differential	200-800mV
TX Amplitude Adjustment	200 mV/step
Pre-Emphasis	6dB
Pre-Emphasis Resolution	20 steps
Equalizing Filter Spacing	-
Total Jitter pk-pk @10G	10 ps (typical)
Total Jitter pk-pk @25G	12 ps (typical)
Rise/Fall Time (20–80%) @25G	17 ps
Sinusoidal Phase Modulation	-
Sinusoidal Jitter Frequency	-
Random Jitter in Phase Modulation	-
Output Return Loss up to 10GHz	< -15 dB
Output Return Loss (16-25GHz)	< -8dB
TX Skew Control Range	-
Lane to Lane Skew Resolution	-
Error Detector Input Amplitude	110-1050 mVpp @11G, 1200 mVpp @25G
Error Detector Maximum Input	1200mV Diff
Error Detector Input Sensitivity	30 mVpp @ 10.3125G / 50 mVpp @ 28G
Phase Scan Resolution	7 bits
Vertical Scan Resolution	8 bits
Input CTLE Dynamic Range	10dB
Reference Clock Output	Rate/32 for 8.5-15G and Rate/80 for 21-30G
Reference Clock Output Amplitude	550-850 mVpp
Reference Clock Input	Rate/32 for 8.5-15G and Rate/80 for 21-30G
Reference Clock Input Amplitude	300-1900 mVpp
Clock Data Recovery	Rate/N (user selectable from 8 and 16)
Power Requirement	12 V dc, 40 W max

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