# **USER GUIDE**



## ML4066 CMIS Analyzer User Guide

CMIS Analyzer Board and CMIS Analysis and Compliance Software| Step-by-Step Guide

User Guide Revision 1.8, July 2021

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# **Revision Control**

Revision number	Description	Release Date
1.0	Preliminary revision	11/27/2017
1.1	<ul> <li>Updated parag 3.2 to match version 1.0 of the GUI</li> </ul>	12/13/2017
1.2	<ul> <li>Adding period selection</li> </ul>	1/4/2018
1.3	<ul> <li>Adding Resistor pullup and Refresh button in cntrl Tab</li> </ul>	4/26/2018
1.4	<ul> <li>Adding application notes</li> </ul>	3/5/2018
1.5	<ul> <li>Update parag 3.3.1</li> </ul>	6/4/2018
1.6	<ul> <li>Add Appendix</li> </ul>	9/4/2019
1.7	<ul> <li>Add CMIS 4.0 State Machine Test</li> </ul>	3/2/2020
1.8	Format Updates	7/27/2021



### Overview

The ML4066 is an adapter with diagnostic interface for the power, I2C and management interface control and alarm signals. The ML4066-ANA analyzer board is connected to the ML4066 to enable live diagnosis for the transceiver and host, ensuring that the entire data was delivered.

The ML4066 also makes use of the Common Management Interface Specification (CMIS) allows host and module software implementers to utilize a common code base across a variety of form factors. CMIS is a robust and increasingly crucial element of data center interconnects, and critical for transceiver stability.



## Analyzer Features

#### **SFF Analyzer features**

- USB Interface
- Windows based GUI and API Library
- Detection and measurement of host pull up + pull down resistors on low-speed signals
- Host VCC rails sampling measurement
- VCC spectral noise analysis
- I2C Analyzer
  - o Bus Speed
  - ACK/ NACK Detection
  - Clock Stretching Analysis
  - o Time Event Logging
- Functional tests
  - o Control signals
  - o Configuration registers
  - $\circ$   $\;$  Ability to emulate optical module by loading identification registers with custom data  $\;$
  - $\circ$  ~ I2C Terminated by microcontroller, I2C slave compliant with MSA
  - $\circ$   $\;$  Implements MSA Memory map and programmable new pages  $\;$
  - o Memory map can be loaded to replicate optical module's identification registers
  - o Ability to control/monitor all low-speed signals
  - o Hot pluggable
- Alarm generation
- State Machine Emulator (CMIS)

#### **CMIS features**

- Communicate with, operate and control various MCBs boards.
- Utilize a common software across a variety of form factors.
- Communicate on multiple host simultaneously, by assigning different USB instance to each host.
- In master mode, the analyzer acts as a host module DUT
  - Load or save MSA files
  - o Read/Write individual module registers
  - o Stretch I2C rate
  - Drive control signals
  - $\circ$   $\;$  State machine sequencing test with transition timing and test report generation
- In slave mode, the analyzer acts as a module for a host DUT
  - Emulate a pluggable full register mapping
  - o Load any MSA file onto analyzer
  - o Clock Stretching during I2C transactions



- Monitor host control signals and raise alarms
- In bypass mode, the analyzer monitors exchange between host and module
  - Analyze and log I2C packet exchange between module and host
  - o Observe control and alarm signal transactions
  - o Monitor VCC levels in real time

#### **SFF Analyzer GUI**

#### VCC tab

The VCC tab allows the measurement of the VCCTX, RX and VCC1. Select the number of samples that will be multiplied by the sampling period selected from the Combo box. The default value of this period is  $0.55 \ \mu$ s.

You can add two markers to the graph by right-clicking with the mouse. Make sure to clear all markers to add new ones.



The values of the markers and their difference are displayed under the graph.

Figure 1: VCC tab



#### I2C Configuration Tab

This tab allows the user to manually configure the I2C bus direction, speed, and clock stretching.

MLAna	alyzer Kit			-	×
<sup>Help</sup> mul	tiL <u>ane</u>	ML4066-Analyzer	Analyzer Type	✓ Disconnect	
Functional Tests I2C Configuration VCC rails	Select I2C Bus Direction: Internal Slave	12C Master Configuration Enable Clock Stretching 12C Speed(10–400KHz) 100 Max 12C Clock Stretching(0–3000us) 1000 Get Apply Configuration			~
• Machine Test Critri/Alrm signals Memory map Fi		r12C Slave Configuration Enable Clock Stretching 12C Clock Stretching(0-225us) 0 Get Apply Configuration			

Figure 2: I2C Capture tab

When choosing Internal Slave, you can Read/Write the Data of the Analyzer's EEPROM. Internal Master allows User to read/write on the Module\*.

Bypass mode makes the communication direct between the module and the host.

For the I2C Master configuration, use the Get button to retrieve the configuration. To change it, write the desired configuration then click "Apply Configuration". The max clock stretching corresponds to the maximum time that the Master waits for the Slave's response. To set the max clock stretching the "Enable Clock Stretching" checkbox must be checked.

For I2C slave configuration, user can choose to enable/disable clock stretching, and can also set the clock stretching time that will be forced on SCL during I2C transactions.

#### Disclaimer:

\*MultiLane supports the replacement of this terminology with more inclusive language. These terms will be retired in the updated CMIS 5.0 specification.

#### I2C tab

This tab analyzes the I2C packets. The graph displays the clock (SCL) and the data (SDA). The SCL rising edges are detected and the SDA values are displayed at each rising edge (cf. image below).



A vertical line is drawn at each rising edge and the SDA binary values are displayed under the yellow SDA curve.

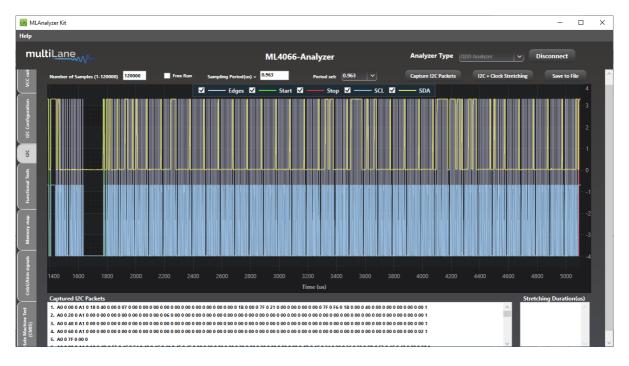


Figure 3: I2C Capture tab

The image above refers to the I2C read command. The data packets are displayed in a list under the graph.

Select the packet that you want to visualize on the graph to see the range of that packet.

Each packet is delimited on the graph by the Start (marked in green) and Stop (marked in red) conditions (cf. image above).

Note that you can show/hide any of the lines by clicking on the corresponding checkbox at the top of the graph.

You can also change the sampling period using the combo box. This period will be multiplied by the number of samples chosen. Its default value is 0.963µs.

To view the reading process, select a higher number of samples so the whole packet can be captured.



Ana	alyzer <mark>Kit</mark>	-																								-		
ıli	tiLane.									м	.4066	-An	alyze	er				A	nalyz	er Type					Dis	connect		
	Number of Sam	ples (1-120000	) 120000		Fre			pling Period					Period							2C Packe	ts	12C +	+ Clock S	Stretchin	g	Save t	o File	
							<u>∽</u> —	— Edges	<b>v</b>		Start	⊻ -		Stop	<b>-</b>	— s	icl 🗹	)  <del></del>	- SDA									
				° (]	•	° (]	。 (]	•	° (]			1	1	1	1 M	L N	°	0 [	0		•	°	•	。 (] ,	• •			
	1000		1040		1060		)80				1140		1160 ne (us)				200	1220		1240		260	1280		1300	132		
	Captured I2C																							5	itretchin	g Durat	ion(us)	
	1. A0 0 7F 0 00 2. A0 0 00 0 A1		2 0 02 0 FF 0	00 0 00	0 00 0 A	0 0 80 0 0	00 0 00 0 0	00 0 00 0 1C	0 75 0	78 0 83	0 00 0 0	0 00 0	00 0 00	0 00 0	00 0 00	0 1E 0 /	A0 0 00 0	00 0 78	0 OF 1									

#### Figure 4: I2C Write

#### Packet Descriptions

Each packet begins with the slave address A0 followed by the acknowledgment 0. The data afterword is the Data Word (7F is the page selection and 00 is the MemPage needed to write on). The second packet presents the writing process on the address 00(hex).

The free run checkbox is used to monitor the I2C bus. When checked, the monitoring function will start sampling directly after the I2C button is clicked.

When unchecked, the monitoring function will automatically detect I2C start frame.

#### Functional Tests Tab

The functional tests tab gives access to the memory pages. You can read/write on registers via I2C using this tab. To read/write from the module, select the "Internal Master" bus direction from the I2C configuration tab, or the "Internal Slave" to read/write from the EEPROM.



Help multiLane ML4066-Analyzer Analyzer Type @DD Analyzer v Disconnect	
	^
	^
12C Read / Write	
O Upper Page 00 O Upper Page 01 O Upper Page 02 O Upper Page 03	
None of the above     Set	
Single Byte	
Address(decimal) Memory Content(Hox) Memory Content(binary)	
Read Write	
Multi-Byte Read	
9 003 07 0000011 9 0000000 9 00000000 9 0000000	
The same to file         004         00         0000000           E         005         00         0000000	
Read         Save to file         004         00         00000000           005         00         00000000         00000000           006         00         00000000         00000000           007         00         00000000         00000000	
6 007 00 0000000 008 00 0000000	
000 00 0000000 010 00 0000000 0 011 00 0000000 0 010 00 0000000 0 0 0000000 0 0 0 0000000 0 0 0 000000	

Figure 5: Functional Tests tab

For the SFP-Analyzer, the functional tests tab adds the slave addresses corresponding to the SFP standards.

MLAnalyzer Kit				- 🗆 X
Help				
multiLane		ML4066-Analyzer	Analyzer Type SFP Analyzer	✓ Disconnect
functional fasts Icc (configuration) VCC-alls	I2C Read / Write Slave Address O Adh A2h Other A0 h Set Single Byte Address(decimal) O Read (Multi Byte Read	Upper Page 03     Vione of the above     Please enter page number  Memory Content(Hed)     Memory Content(Hed)     00000011	Upper Page 02 Set	
Memory map	Starting Address (Dec) End A	001 04 0	Binary 00000011 ^ 00000100	
State Machine Test Catridates signals	Read Sa	ave to file 003 11 0 084 00 0 005 00 00 007 00 00 007 00 00 008 04 0 010 00 0	□ 00000000 □ 00000000 □ 00000000 □ 00000000 □ 00000000 □ 00000000 □ 00000000 □ 00000000 □ 00000000 □ 00000000 □ > ↓	

Figure 6: Functional Tests Tab for SFP-Analyzer

#### I2C Read/Write:

- 1. First, select which page you need to perform a read or write operation on in the Memory Location.
- 2. Then, use the "Single Byte" window to read/write one byte from the memory.
  - a. Address: The address to read/write from.



- b. Memory Content: The data value to be read/written to the selected address (In Hex or in Binary).
- 3. Alternatively, use the "Multi-byte Read" to read/write multiple bytes between a specified Starting Address and an End Address.

#### Memory Map Tab

This tab gives access to the memory map of the module. It can be loaded to replicate optical module's identification registers.

MLAnalyzer Kit								-	×
Help									
multiLane				ML40	66-Analy	zer Analyzer	Туре	Disconnect	
VCC rails		Refresh	Load M	6A from file	Save	MSA to file Write MSA to HW			Â
ACC 1		Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description	1		
, <u>p</u>	Þ	LowMem 0(00h)	18	24	٥	Identifier	1		
guratio		LowMem 1(01h)	40	64	0	Version Id			
I2C Config		LowMem 2(02h)	00	0		CLEI code present			
120.0		LowMem 3(03h)	07	7	٥	Module State			
		LowMem 4(04h)	00	0		Bank 0			
Z		LowMem 5(05h)	00	0		Bank 1			
		LowMem 6(06h)	00	0		Bank 2			
Tests		LowMem 7(07h)	00	0		Bank 3			
oual		LowMem 8(08h)	00	0		Module State changed flag			
		LowMem 9(09h)	00	0		Latched VCC3.3/Temp Alarm and Warning			
<u> </u>		LowMem 10(0Ah)	00	0		Latched AUX1/2 Alarm and Warning			
dem		LowMem 11(0Bh)	00	0		Latched Vendor Defined Alarm and Warning			
		LowMem 12(0Ch)	00	0		Reserved			
Memory		LowMem 13(0Dh)	00	0		Custom			
2		LowMem 14(0Eh)	1C	28		Internally measured Temperature 1 MSB			
<u> </u>		LowMem 15(0Fh)	00	0		Internally measured Temperature 1 LSB			
signs		LowMem 16(10h)	7F	127	1	Internally measured Supply 3.3v MSB			
E .		LowMem 17(11h)	OB	11	0	Internally measured Supply 3.3v LSB			
Cutri/Airm sig		LowMem 18(12h)	00	0		Internally measured AUX1 MSB			
		LowMem 19(13h)	00	0		Internally measured AUX1 LSB			
T		LowMem 20(14h)	00	0		Internally measured AUX2 MSB			
ne Test		LowMem 21(15h)	00	0		Internally measured AUX2 LSB			
Machin CMIS)		LowMem 22(16h)	7F	127	1	Internally measured AUX3 MSB			
		1 22/17h)		220	2	Informative management AUX21CD	-	 	 $\sim$

Figure 7: Memory Map tab

This screen allows you to Load or Save your custom MSA configuration.

Data is displayed according to the selected I2C Bus Direction in a grid showing: register address,

hex value, Decimal Values, ASCII value, MSA description.

- **Refresh** button: Read MSA Registers, and refresh values.
- Write MSA to HW button: Write the current MSA configuration to OSFP module.
- Save MSA to file button: Saves the current MSA memory to a file using Comma separated values (CSV) format.
- Load MSA from file button: Loads MSA values from file and map it to MSA memory.

When choosing **Internal Slave**, you can Read/Write the Data of the Analyzer's EEPROM. **Internal Master** allows you to read/write on the Module. **Bypass mode** makes the communication direct between the module and the host.



For the SFP-Analyzer, choose your desired slave address and page to read it.

💼 MLAnaly Help	/zer Kit							 -	
	iLane			ML40	66-Analyz	er	Analyzer Type	Disconnect	
VCC rails	Choose addresses to display Slave address A0 V	Refresh	Load MS	A from file	Save	MSA to file	Write MSA to HW		
<u>&gt;</u>		Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description	<b>^</b>		
5		S.A. A0 Byte 0 (00h)	0	0	0	Identifier			
purati		S.A. A0 Byte 1 (01h)	0	0	0	Ext. Identifier			
Configuration		S.A. A0 Byte 2 (02h)	0	0	0	Connector			
ISC C		S.A. A0 Byte 3 (03h)	0	0	0	Transceiver			
		S.A. A0 Byte 4 (04h)	0	0	0	Transceiver			
IZC		S.A. A0 Byte 5 (05h)	0	0	0	Transceiver			
		S.A. A0 Byte 6 (06h)	0	0	0	Transceiver			
Functional Tests		S.A. A0 Byte 7 (07h)	0	0	0	Transceiver			
onal		S.A. A0 Byte 8 (08h)	0	0	0	Transceiver			
uncti		S.A. A0 Byte 9 (09h)	0	0	0	Transceiver			
-		S.A. A0 Byte 10 (0Ah)	0	0	0	Transceiver			
		S.A. A0 Byte 11 (0Bh)	0	0	0	Encoding			
Memory map		S.A. A0 Byte 12 (0Ch)	0	0	0	BR, Nominal			
hou		S.A. A0 Byte 13 (0Dh)	0	0	0	Rate Identifier			
Me		S.A. A0 Byte 14 (0Eh)	0	0	0	Length(SMF,km)			
		S.A. A0 Byte 15 (0Fh)	0	0	0	Length(SMF)			
se		S.A. A0 Byte 16 (10h)	0	0	0	Length			
Cntrl/Airm signals		S.A. A0 Byte 17 (11h)	0	0	0	Length			
Alm		S.A. A0 Byte 18 (12h)	0	0	0	Length			
		5.A. A0 Byte 19 (13h)	0	0	0	Length			
<u> </u>		S.A. A0 Byte 20 (14h)	0	0	0	Vendor Name			
Ĩ		5.A. A0 Byte 21 (15h)	0	0	0	Vendor Name			
ine (		S.A. A0 Byte 22 (16h)	0	0	0	Vendor Name			
CMIS		5.A. A0 Byte 23 (17h)	0	0	0	Vendor Name			
State Machine Test (CMIS)			1						
N.									

Figure 8: Memory Map tab in SFP analyzer

#### CNTRL/ALRM Signals tab

This tab allows detection and measurement of host pull up resistors on low speed signals and the detection of their state (either digital or analog). You can also drive these signals using the corresponding checkboxes.

- Pull-Up Resistors window: The analyzer detects if the pull-up resistor of each signal is missing or not and it calculates its value. The range between 1.3 KΩ and 10 KΩ is acceptable indicating that a pull-up resistor is present. Below 1.3 KΩ the resistor value is too low and you a short circuit. Above 10 KΩ you risk an open circuit. The marge of accuracy for the resistor's value is about 1 KΩ.
- For each signal the desired mode "Drive", "Bypass" or "Analog Sampler" is chosen. The Analog Monitor button displays the voltage of the desired signal. To manually assert/deassert the signals, the "Drive" option must be chosen to be able to toggle the signal's checkbox. Finally, if "Bypass" mode is selected, you can control the module externally and check its status by pressing the "Get" button.
- The Refresh button resets the signals in "Drive" mode to their initial states.



MLAnalyzer Kit		– 🗆 X
Help		
multiLane	ML4066-Analyzer Analyzer Type	Disconnect
VCC raft	Analog Monitor:	^
ACCE	ResetL	4
INPUT:		3.5
5 Mode: Drive ✓		3
		2.5
		2 ¥
2. Intrivide angital 3. Analog Monitor		1.5
		1
ModSelL [ResetL]		0.5
Mode: Bypass V Mode: Analog Sampler V		0.5
2 1. ModSell 1. T Resetl		800
2. ModSetL digital     2. ResetL digital     3. Analog Monitor     3. Analog Monitor	Time (us)	
	م Pull-Up Resistors	
OUTPUT:	Refresh VCC VCC VCC	vcc
	Resistor pulled up	
Mode: Bypass V Mode: Bypass V	Resistor value too low	
1.     IntL     1.     ModPrsL       3     2.     IntL digital     2.     ModPrsL digital	4.244 K 4.273 K 1.766 K	1.766 K
1. I intt 2. O intt digital 3. Analog Monitor I. ModPat 2. ModPat 3. Analog Monitor	ModPrsL IntL I2C SCL	I2C SDA

Figure 9: Cntrl/Alrm signals tab 1 in QDD analyzer

The pin pull-up resistors will differ depending on the form factor of the adaptor and module.

MLAnalyzer Kit Help		-	
multiLane	ML4066-Analyzer	Analyzer Type SFP Analyzer V Disconnect	
Very regregation     0     : Signal is High.     : Signal is Low.     Refrech.       OUTPUT:     The Signal is Low.     Refrech.     Image: Signal is Low.     Refrech.       The Signal is High.     . Signal is Low.     NPUTD.     Image: Signal is Low.     Refrech.       The Signal is High.     . Signal is Low.     NPUTD.     Image: Signal is Low.     NPUTD.       The Signal is High.     . Signal is Low.     NPUTD.     Image: Signal is Low.     NPUTD.       The Signal is Low.			10 9 8 7 6 5 00 4 - 3 - 2 1 0
2.     Rx LOS digital       3.     Analog Monitor       1.     Image: Solution of the	Pull-Up Resistors Refresh VCC Refresh VCC Resistor pulled up Resistor value too how Resistor value too high Resistor value too high Resistor value too high	Time (us)	

The SFP has different low speed control signals as seen in the figure below.

Figure 10: SFP-Analyzer Control signals

#### **Application Notes**

#### I2C Tab

1. Select "Bypass" mode from the "I2C Configuration" tab.



- 2. In the I2C tab, select the number of samples for the I2C capture, for the I2C read itshould be the maximum.
- 3. Without selecting the "free run" checkbox, click the I2C button to start monitoring, then using your host send an I2C command (read or write) and wait for the I2C Frame Capture.
- 4. If the "free run" checkbox is selected, the capturing will start immediately after the I2C button is clicked.

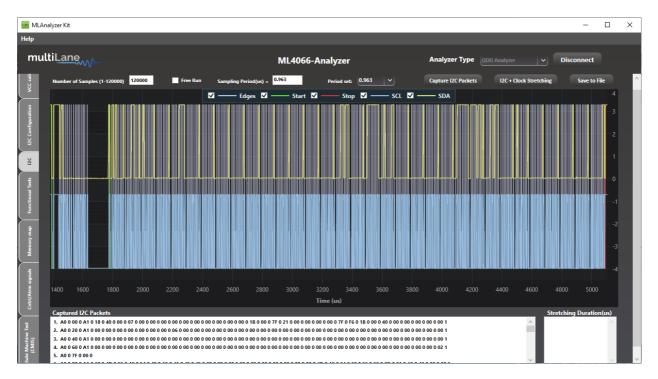


Figure 11: I2C Read

#### Functional Tests Tab

1. Select "Bypass" mode in the I2C configuration tab, using your host try to read/write a value from the module. In the Analyzer GUI, the read/write won't work in this mode because the Host and module communicate directly without the interference of the Analyzer.



MLAnalyzer Kit				– 🗆 X
Help				
multiLane		ML4066-Analyzer	Analyzer Type SFP Analyzer	<ul> <li>✓ Disconnect</li> </ul>
functional Tech. Its Configuration VCC with	O A0h ● A2h ● Other A0 h Set Single Byte Addres(decimal)	Memory Location Upper Page 03 Upper Page 03 None of the above Memory Context(Hea) Upper C		
State Machine Tel Cett/Aven signals Memory may (AMS)	Starting Address (Dec) End Add	tex (bec) Addres Hex 000 03 001 04 002 00 003 11 004 00 005 00 005 00 005 00 005 00 005 00 006 04 009 00 010 00 011 00 100 02 000 03 000 00 000 000	Binary 0000011 0 0 0000000 0 0000000 0 0000000 0 000000	

Figure 12: Functional Tab in Master Mode

 Select "Internal Master" mode in the I2C configuration tab, read address 0 using the Analyzer GUI. This value refers to the one written on the module. The connection between the Host and the Analyzer is cut and using the Host to read will give you FF values.

MLAnalyzer Kit				– 🗆 X
Help				
multiL <u>ane</u>	ML4066-A	Inalyzer	Analyzer Type QDD Analyzer	<ul> <li>✓ Disconnect</li> </ul>
tractional Tata. DC Configuration VC rais	I2C Read / Write  Memory Location  Upper Page 00 Upper Page 01 Upper None of the above  Single Byte  Address(decimal) Memory Content(Hea)  Read	er Page 02 Upper Page 03 Set Memory Content(binary) 00011000 Write		
Machina Tat Catolian spak Mamon mp	Mutti Byte Read Starting Address (Dec) End Address (Dec) C 100 Read Save to file	Address         Hex         Einur           000         18         00011000         0000000           002         00         00000001         0000000           002         00         00000001         0000000           005         00         00000000         000           005         00         00000000         000           007         00         00000000         000           007         00         00000000         000           007         00         00000000         000           007         00         00000000         000           007         00         00000000         000           007         00         00000000         000           010         00         00000000         011           00         00000000         011         00         00000000	× • • • •	

Figure 13: Functional Tab in Slave Mode

3. Select "Internal Slave" mode in the I2C configuration tab, the reading/writing command from the Analyzer or your Host will give the same value written in the EEPROM.



MLAnalyzer Kit		- 🗆 X
Help		
multiLane	ML4066-Analyzer Analyzer Type	r V Disconnect
DC RC Configuration VCC rafk	I2C Read / Write Slave Address Adh Azh Other A0 h Set Single Byte Single Byte	
functional tests IX	Address(decimal) Memory Content(Hea) Memory Content(Disary) 0 03 0000011 Read Write	
Atemos rado	Starting Address (Dec)         End Address (Dec)         Address         Here         Binary           0         100         000         02         00000011         000           001         04         00000100         000         000         000	
Critr/Atm signals	Read         Save to file         003         11         0010001           004         000         00000000         0           005         00         00000000         0           006         00         00000000         0           007         00         00000000         0           008         04         00000000         0           008         04         00000000         0           009         00000000         0         0	
State Machine Test (CMS)		

Figure 14: Reading Specific Registers from Functional Tests Tab

When clicking "Refresh" in the "Memory Map" tab, the grid displays all data written in the registers and follows the rules above.

MLAnalyzer Kit								-	
Help									
multiLane				ML40	66-Analy	zer Anal	yzer Type	Disconnect	
VCC raits		Refresh	Load MS	SA from file	Save	MSA to file Write MSA to I	łW		
<u> </u>		Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description	<b>_</b>		
ation	►	LowMem 0(00h)	18	24	0	Identifier	_		
figura	l	LowMem 1(01h)	40	64	0	Version Id			
		LowMem 2(02h)	00	0		CLEI code present			
12C Coi	L	LowMem 3(03h)	07	7	0	Module State			
		LowMem 4(04h)	00	0		Bank 0			
12C		LowMem 5(05h)	00	0		Bank 1			
		LowMem 6(06h)	00	0		Bank 2			
al Tests		LowMem 7(07h)	00	0		Bank 3			
leno		LowMem 8(08h)	00	0		Module State changed flag			
uncti	L	LowMem 9(09h)	00	0		Latched VCC3.3/Temp Alarm and Warning			
<u></u>		LowMem 10(0Ah)	00	0		Latched AUX1/2 Alarm and Warning			
de		LowMem 11(0Bh)	00	0		Latched Vendor Defined Alarm and Warning			
ory m		LowMem 12(0Ch)	00	0		Reserved			
Memo		LowMem 13(0Dh)	00	0		Custom			
2		LowMem 14(0Eh)	1C	28		Internally measured Temperature 1 MSB			
- Se	L	LowMem 15(0Fh)	00	0		Internally measured Temperature 1 LSB			
ling		LowMem 16(10h)	7F	127	1	Internally measured Supply 3.3v MSB			
Cntrl/Alrm sig		LowMem 17(11h)	0B	11	0	Internally measured Supply 3.3v LSB			
ntr//		LowMem 18(12h)	00	0		Internally measured AUX1 MSB			
		LowMem 19(13h)	00	0		Internally measured AUX1 LSB			
ŭ		LowMem 20(14h)	00	0		Internally measured AUX2 MSB			
		LowMem 21(15h)	00	0		Internally measured AUX2 LSB			
MIS)	L L L	LowMem 22(16h)	7F	127	1	Internally measured AUX3 MSB			

Figure 15: Internal Master

#### Cntrl/Alrm Tab

1. The refresh button gets the Status of the signals at the "Drive" mode and the checkboxes reflect its condition.

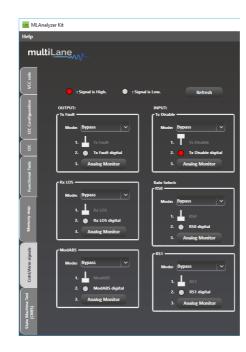


Figure 16: Cntrl/Alarm Tab

- 2. Select "Drive" mode for ResetL and toggle the checkbox, the ResetL signal of the module will be activated or deactivated.
- 3. Select "Bypass" mode, from Host try to trigger the ResetL signal. Check the analyzer GUI's status by clicking on "Get" button.
- 4. Select "Analog Monitor" mode and click on the "Analog Monitor" button of ResetL. The graph displays its DC voltage level from the Host side.



Figure 17: Reading ResetL from the Analog Monitor Window

multiLane



5. In the "Pull-Up Resistors" Groupbox, click the "Refresh" button, the values displayed are the values of the pullup resistors at the Host.

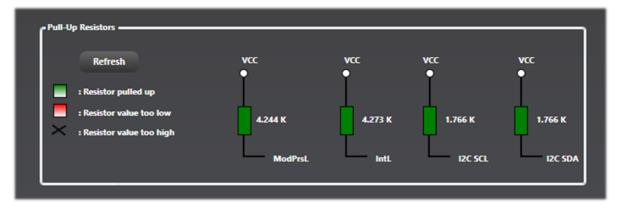


Figure 18: Pull-Up Resistor Values



## CMIS State Machine Test

This analyzer test works for all QSFP and QDD modules that are both CMIS 3.0 and CMIS 4.0 compliant. In CMIS 3.0, the test skips the low power if the configuration is set to high when transitioning from state to state. In CMIS 4.0, the transition passes through the low power configuration to get to high power.

The Module State Machine is engaged after module insertion and power on, and thus the test can be started. During the test, different state transitions can be shown and tested by toggling the desired destination state. The Module State Machine is different for devices implementing a paged memory map and those implementing a flat (non-paged) memory map.

MLAnalyzer Kit				-		×		
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VCc.mk								
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77								
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dem Viol	It will switch to its previously set mode when the test is stopped. Initialize Test							
Mean Market Market								
Call () Rhum signais								
State Machine Test (CMIS)								

Figure 19: Landing Page for State Machine Test

Upon test initialization, the CMIS compliance version is verified and module type is detected. If the latter is not feasible the test will not start.

#### **Paged Memory Modules**

If the detected module implements a paged memory map, the diagram below appears and displays the current state of the module and the transition signals.

Toggle another steady state (Reset, ModuleLowPwr, ModuleReady) to switch to it. State and transition signal changes will appear and events will be logged in the logging box. Logged events can be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be thrown into a "Fault" state. This state can be exited only by resetting the module.





Figure 20: State Machine Test for Paged Memory Modules

#### **Flat Memory Modules**

If the detected module implements a flat (non-paged) memory map, the diagram below appears, displaying the current state of the module and the transition signal.

Toggle any of the steady states (Reset or ModuleReady) to switch between them. State and transition signal changes will appear and events will be logged in the logging box. Logged events can be saved to a text file possessing the module serial number and the time the test was done.

If an error occurs while transitioning, the module will be stuck in the transition state until resetting the module or re-initializing the test.

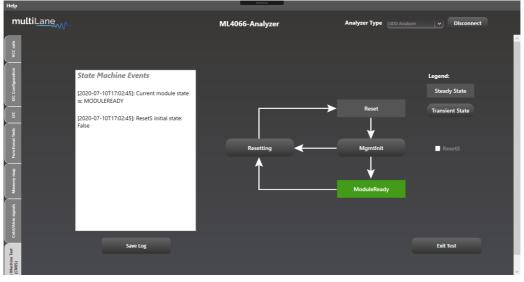


Figure 21: State Machine Test for Flat Memory Modules



# Appendix I: Analyzer Card Diagram

