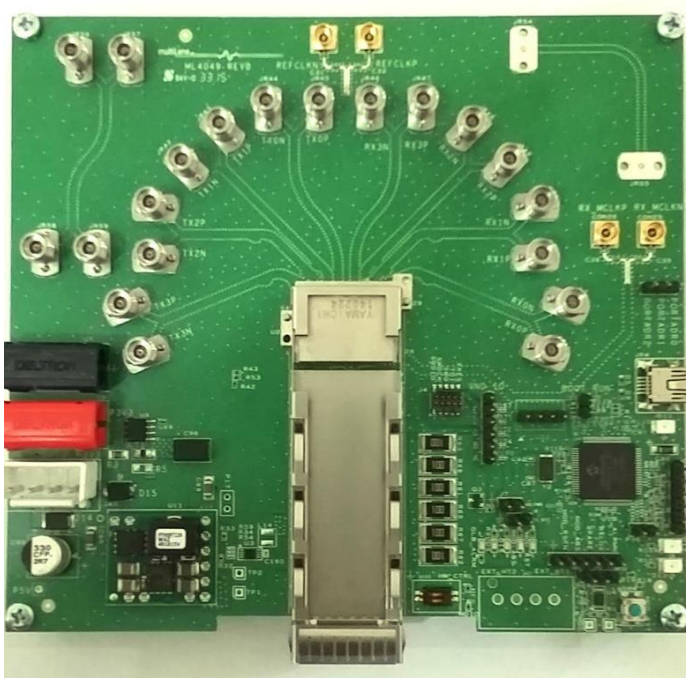
ML4049

MSA Compliant

CFP4 MCB



Revision 0.1

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multiLane

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1. General Description

CFP4 MSA Compliant Host board ML4049, is designed to provide an efficient and easy method of programming and characterizing CFP4 transceivers.

The ML4049 comes complete with a user friendly GUI supporting all features defined by CFP4 MSA and user manual to enable intuitive testing. Current sense capability is also included in the Host. It is equipped with AOC testing capability for performing 4-corner testing.

2. ML4027-ACO CFP2-ACO test board - Key Features

- ✓ High Performance signal integrity traces from edge connectors to CFP4 host connector
- ✓ CFP4 MSA Form Factor
- ✓ 40 GHz Bo-Jiang 2.92mm K Connectors
- ✓ MDIO MSA compliant master
- ✓ Matched differential trace length
- ✓ Supports 4x28G interfaces
- ✓ All 4 channels comes with matching trace length
- ✓ On-board LEDs showing MSA output Alarm states
- ✓ On-board buttons/jumpers for MSA input control signals
- ✓ USB interface
- ✓ CFP4 Host/ Module Status and control
- ✓ User friendly GUI for MDIO control and loading custom MSA Memory Maps

3. Operating Conditions

Recommended Operation Conditions						
Parameter	**Symbol**	**Notes/Conditions**	**Min**	**Typ**	**Max**	**Units**
Operating Temperature	T_A		0		85	°C
Supply Voltage	VCC	Main Supply Voltage (from external PS)	3.00	3.3	3.60	V
Supply Voltage	VCC	Supply voltage from DC adapter		5		V

3.1. LEDs

The LED D11 indicates whether a USB cable is plugged or not.
The other two LEDs, D12 and D13, are used for diagnostic purposes.

- If the green LED, D13, is on: USB is locked and device is recognized by the USB driver.
- If the red LED, D12, is on: USB not connected or USB driver not found.
- If both LEDs are off: Board not powered correctly or firmware is corrupted.

4. Power Supplies

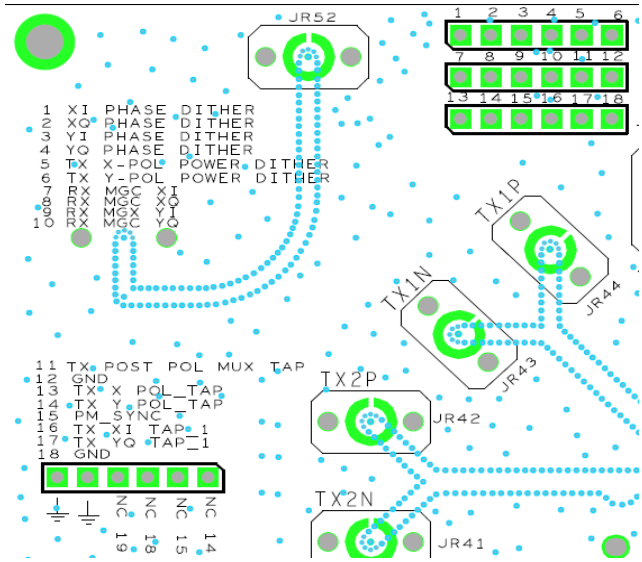
The board can be powered using a 3.3V external power supply through banana plugs U6, U7, or using a 5V DC adapter jack with J2.

A current sense is available on the board, and it measures the current draw on the main P3V3 net.

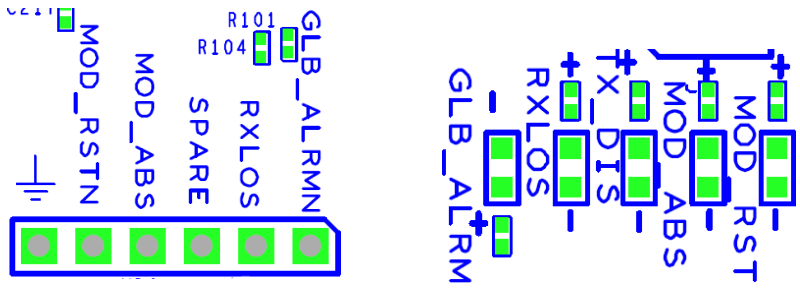
5. CFP4 HW Signaling Pins

Hardware alarm pins, hardware control pins and MDIO pins can be accessed from the software via USB or through on-board LEDs and pin headers. Dip switch U153 allows switching signaling pins control between software and hardware.

Access to all ACI signals is provided by the pin headers shown below:

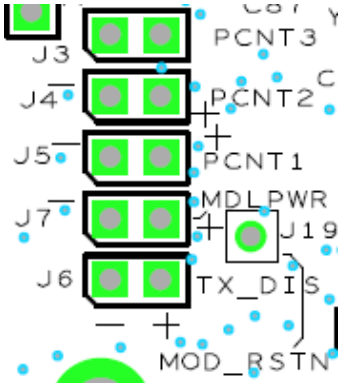


All Hardware Alarm signals can be accessed through the pin headers or LEDs shown below:

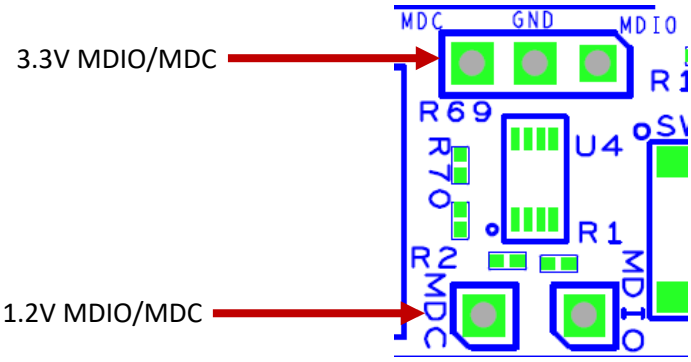


Note that D16 shows the state of GLB_ALRM signal which is the inverse of GLB_ALRMn pin.

All hardware control signals can be driven through the jumpers shown below:



Below are the pin headers for the MDIO interface:



6. High Speed Signals

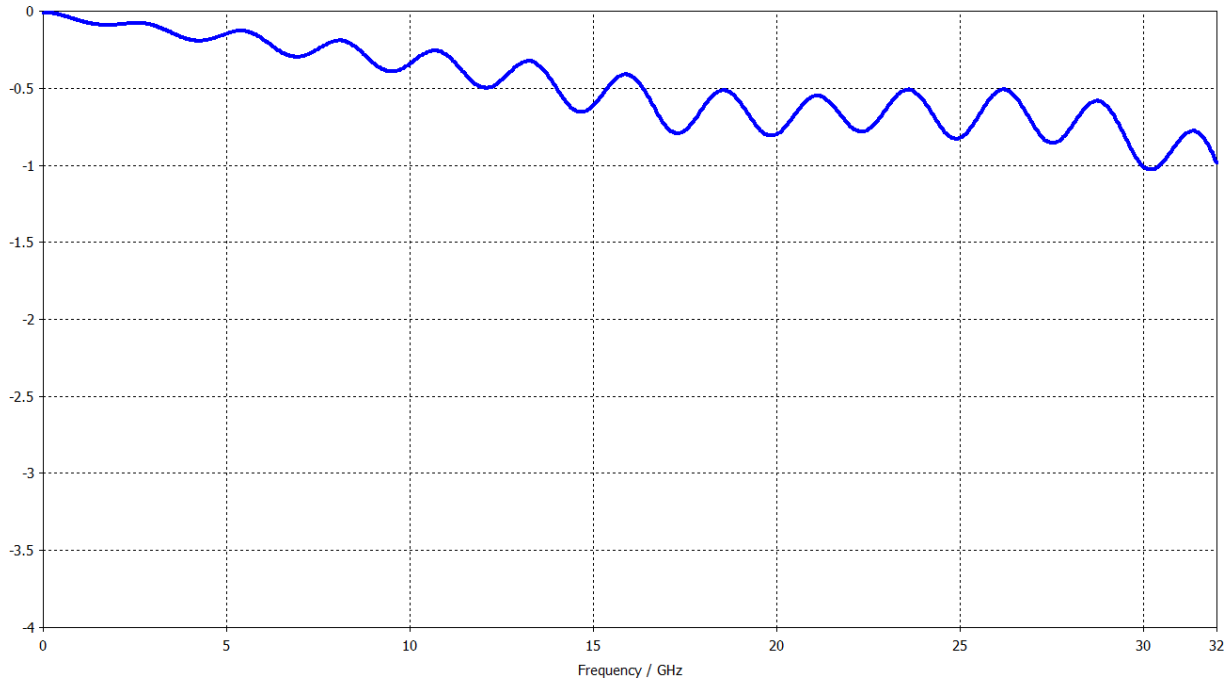
6.1.1. S-Parameters

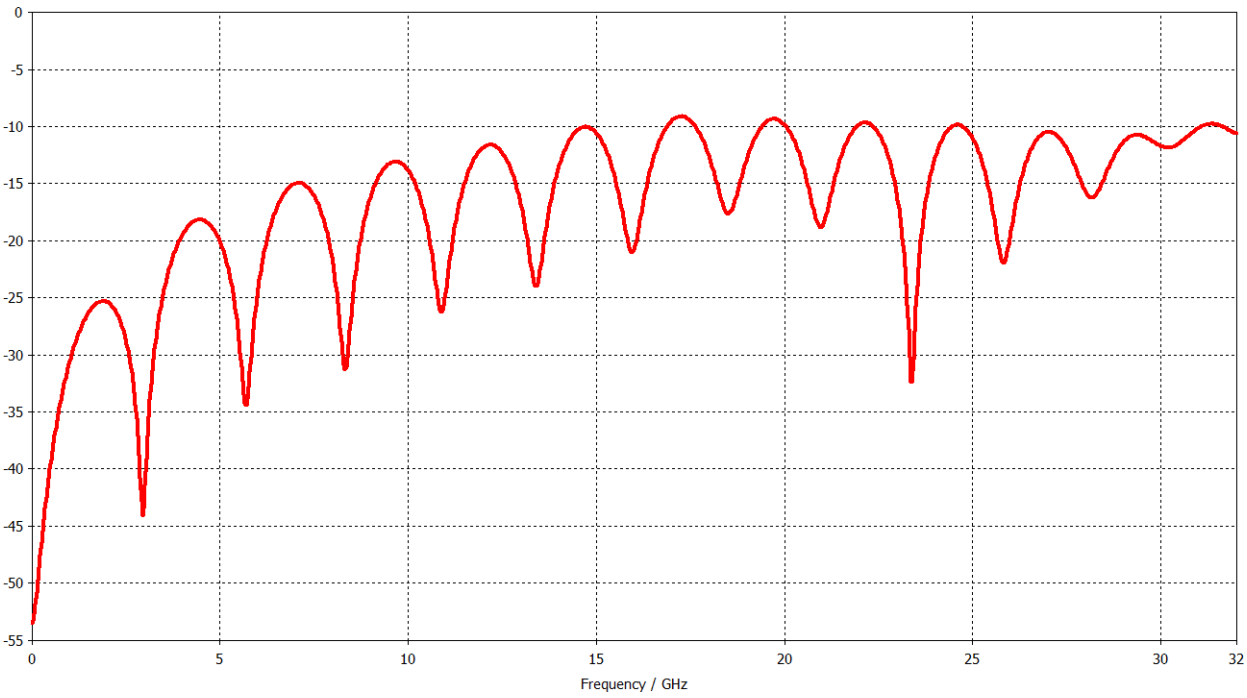
All TX and RX channels on the board have the same trace length and geometry. A differential test trace of same length and geometry as the channels is available on the board to be used for de-embedding the MCB traces from the measurements.

Simulated S4P files for all the channels are available on the following link:

https://www.dropbox.com/sh/aq8gvtwx8tzn2xx/AABWQP9Uq8KxpyCP89ns7FQaa/CFP2%20ML4027-ACO-MCB/S4P?dl=0

Below are the insertion loss and return loss graphs for channel RX3:





6.2. Reference Clock

REFCLK N/P, TX_MCLK N/P and RX_MCLK N/P are accessible through SMP connectors and are AC coupled.

7. Installation

7.1. USB Driver Installation on Windows XP

The USB driver files are as shown below:

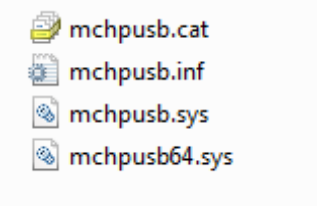


Figure 1: USB driver files

- Power on the CFP4 Host fixture.
- Plug-in the USB cable into the PC and connect it to the CFP4 Host fixture.
- The following window will pop up.
- Choose the "**No, not this time**" option, and then click "**Next**".

Figure 2: USB driver installation

- Choose "**Install from a list or specific location (Advanced)**", and then click "**Next**".

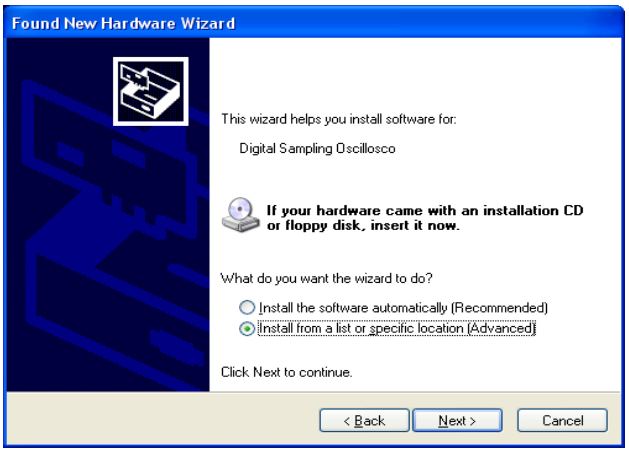


Figure 3: USB driver installation Advanced

- Choose “**Search for the best driver in these locations**”.
- Check the choice: “**Include this location in the search**”.
- Browse for the subfolder: “**CFP Host**” existing in “**MultiLane Drivers**” folder in the installation path (this is customized).
    - Choose it and then click **“Ok”**.
- Click “**Next**”.

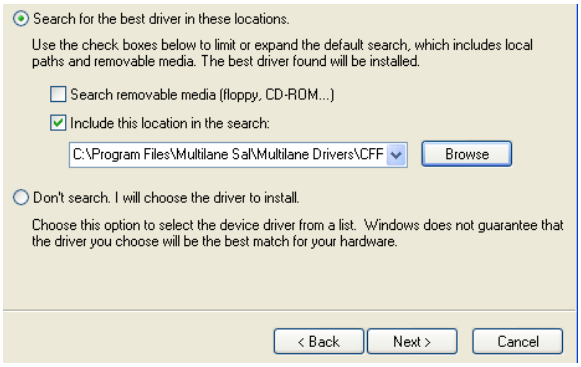


Figure 4: USB driver location

Figure 5: USB driver folder

- When this window appears, click “**Finish**”. The USB driver is now installed.

Figure 6: USB driver installation Finish

7.2. USB Driver fix for Windows 8

Temporarily disable Windows 8 "Driver Signature Enforcement":

a. Select "Settings" for the right side menu, then "Change PC settings"
b. Under the "General" tab, scroll down to "Advanced startup" and click on "Restart now" as shown in Figure 7 below.

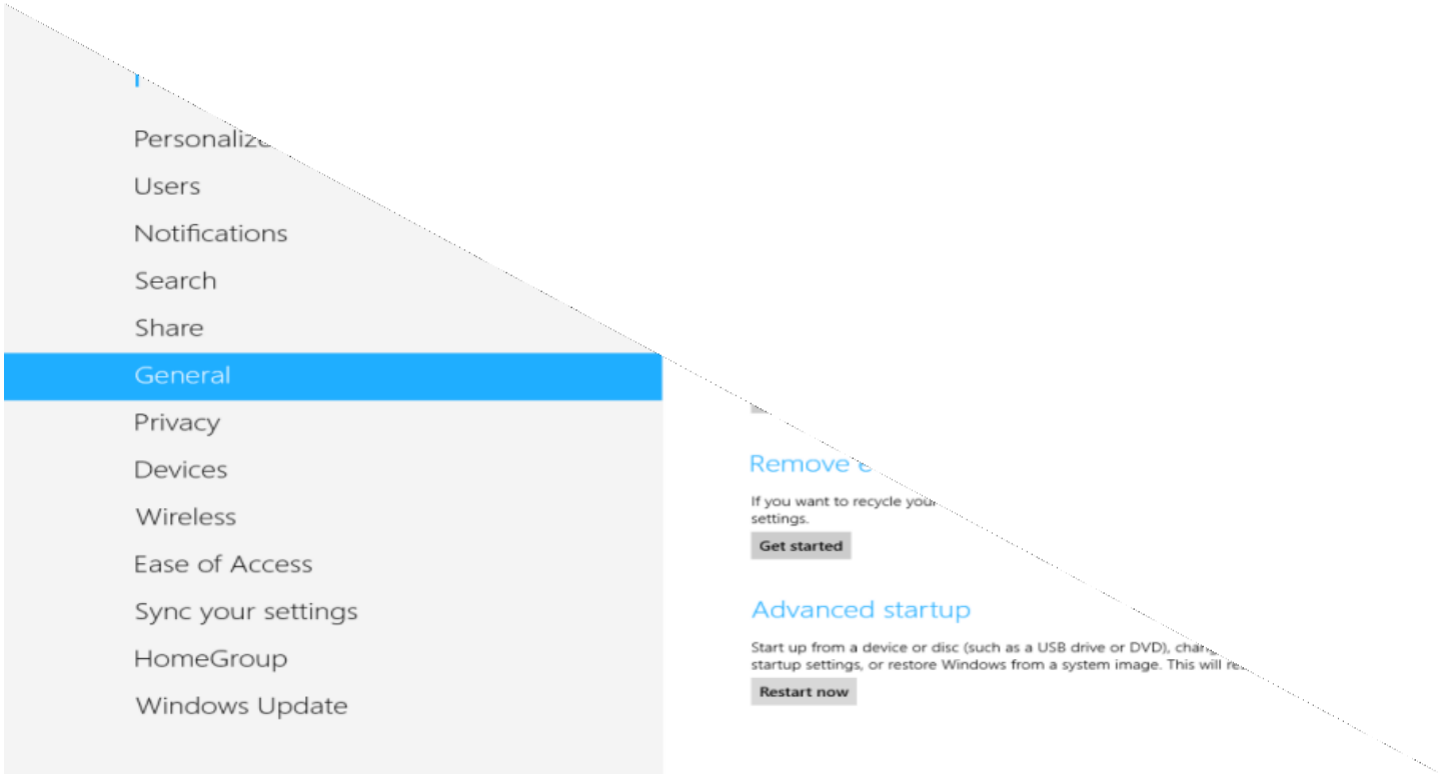


Figure 7: PC settings

c. Select "Troubleshoot/Advanced options/Startup settings/Restart"
d. Press "F7" for the "7) Disable driver signature enforcement"

Install the MCHPUSB driver manually from MCHPUSB.inf ("Install this driver software anyway")

Control Panel

a. Open "Device manager" from the "Control panel"
b. Right click the unrecognized device and select "Update driver software"
c. Select "Browse my computer for driver software"
d. Select "Let me pick from a list of device drivers on my computer"
e. Select "Custom USB device"
f. Select the corresponding model (Microchip Custom USB Device)

7.3. Communication Window

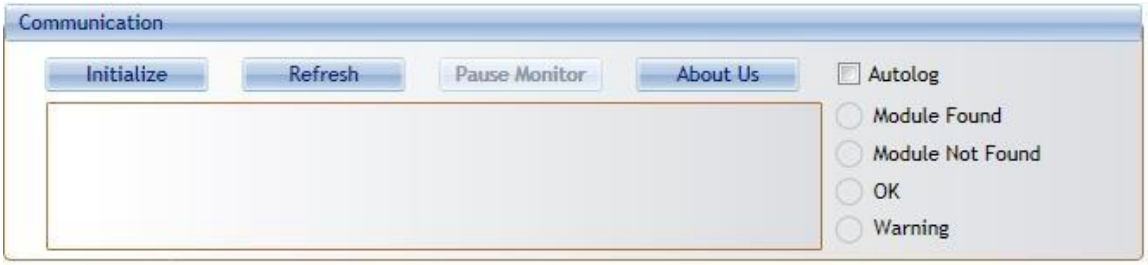


Figure 8: Communication Window; Main Interface used for initial communication with host

7.3.1. Initialize button

It's the application's main entry point, used to establish a connection with the CFP4 Host board and the Module. Once a USB connection is established, the Host checks if a CFP4 Module is inserted, and accordingly illuminates the corresponding (Module Found or Module Not Found) LED. If a CFP4 Module is inserted, the initialization process proceeds with the MSA compliant startup sequence for the module as shown in the diagram below:

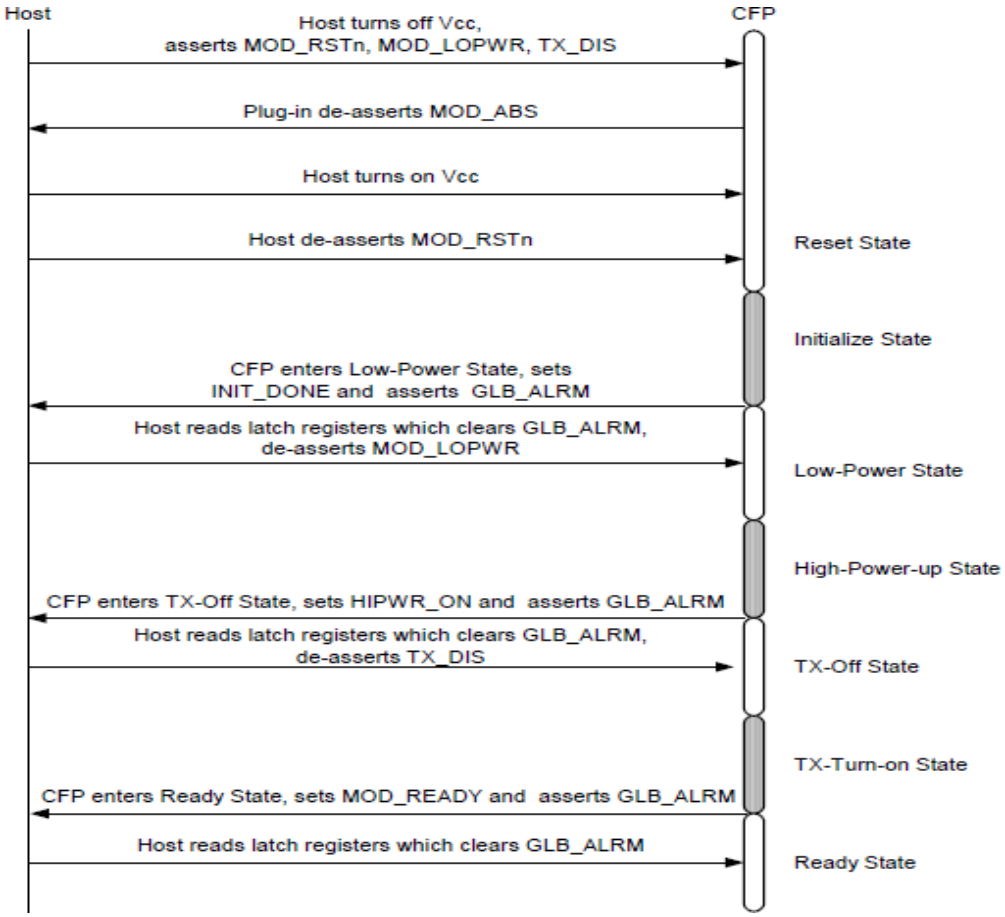


Figure 9: MSA Compliant Startup Sequence

Hence, the CFP4 module goes through Reset, Initialize, High-Power up, TX-Off, TX-Turn-on states, and finally enters the Ready state. During this sequence, the CFP4 module sets INIT_DONE, asserts GLB_ALRM, HIPWR_ON, and MOD_READY signals sequentially. These signals inform host the completion of control circuit initialization and MDIO availability, module fully powered up, and module ready for data, respectively. **OK** LED will be asserted when the module startup sequence is complete.

Next, the status box window in the GUI will show any success or failure messages that are being returned as a result of the GUI communicating or attempting to communicate with the hardware.

Figure 10: Communication status box showing a connection error

The above figure shows a typical connection error when a connection attempt with the host fails. The default Error Status format is: [funtion]:[returned error].

The picture below shows how the status box should appear after a successful connection.

Figure 11: Communication status box showing successful connection

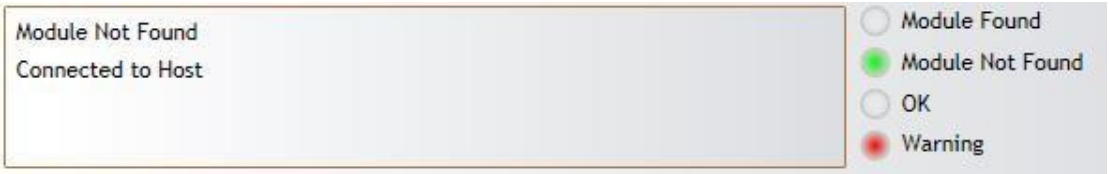


Figure 12: Communication status box when connected to host but no module is plugged

Please note that the status box messages are always shown with the most recent message on top. You can check the “Autolog” check box for activating the silent logging mode. In this mode, a log file will be automatically generated, and all software steps will be logged during runtime and is useful for debugging purposes when communicating with Multilane applications engineering support.

7.3.2. Refresh button

Checks for connection status, refreshes Hardware Readings and updates GUI.

7.3.3. Pause Monitor button

Pauses or resumes monitoring.

7.3.4. About Us button

Shows program information (name, version) and company information.

7.4. Graphical User Interface Section

The GUI for the CFP4 host board contains 12 sections giving the user the ability to monitor, customize, control and configure the Hardware.

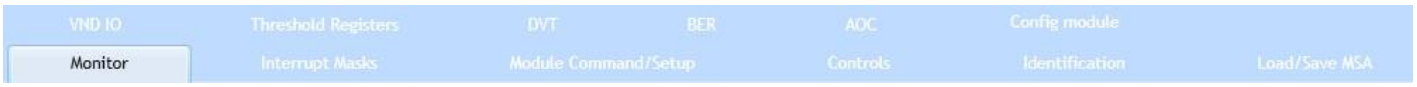


Figure 13: GUI tabs

As shown in Figure 13 above, the GUI contains the following main tabs:

- ✓ **Monitor**: Monitoring interface allowing the user to check the Hardware operation (selected by default).
- ✓ **Interrupt Masks**: Allows the user to select which FAWS bits to contribute to GLB_ALRM.
- ✓ **Module Command/Setup**: Allows the user to control module behavior.
- ✓ **Controls**: Provides both additional and alternative controls to hardware pins and programmable control pins in controlling CFP4 module.
- ✓ **Identification:** Shows module Base ID Registers.
- ✓ **Load-Save MSA/Load-Save MSA ACO:** Save the current CFP4 configuration to a file, or load existing configuration from file and map it to MSA memory.
- ✓ **VND IO:** Provides control for CFP Vendor IO pins.

7.4.1. Monitor

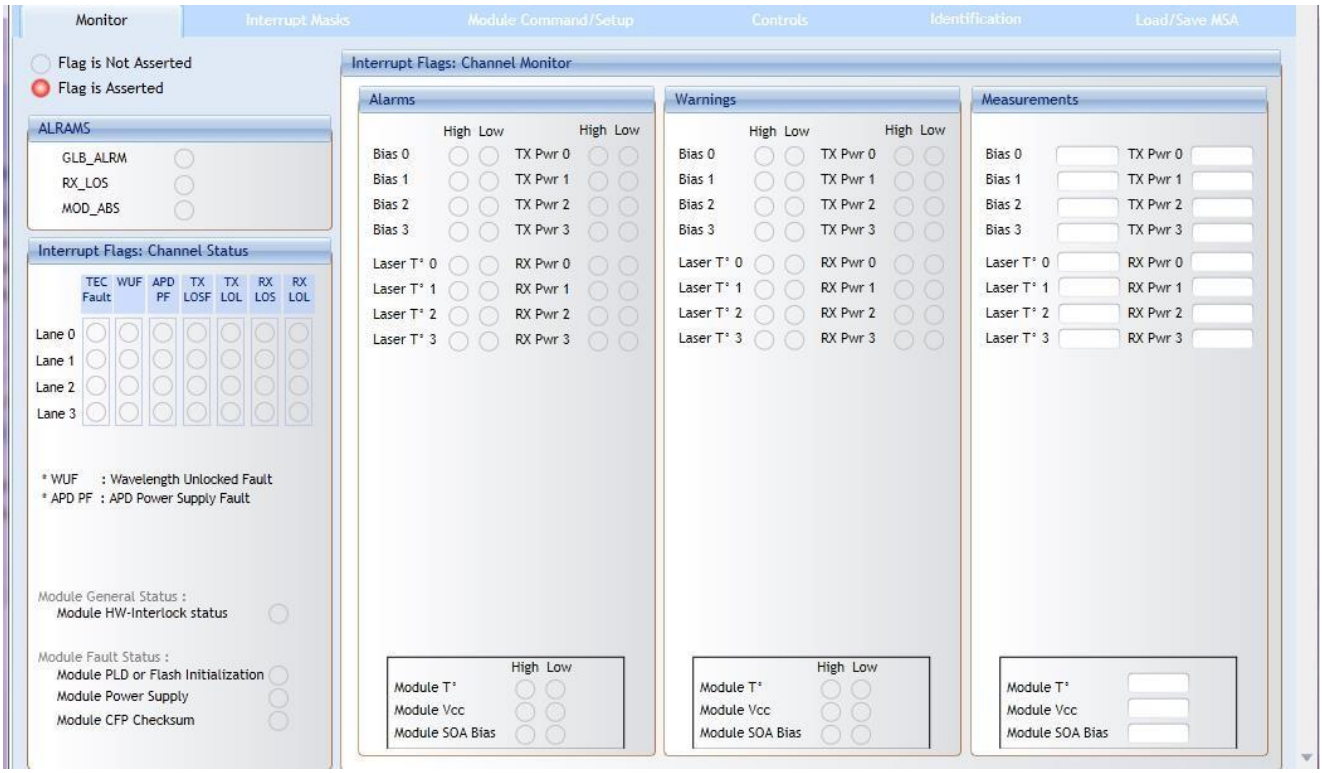


Figure 14: Monitor Window

Digital Diagnostic Monitor:

The Monitor Window shown in Figure 14 above is the main source of the module status and alarm/warning flags conditions. It shows the current status of a flag, the default flag update rate is 2 Hz, so the flag status is updated every 0.5 seconds.

Flag Status:

- Flag is not asserted: the corresponding LED is OFF (Transparent).
- Flag is asserted: the corresponding LED is ON (Red).

The Monitor window shows 3 different sections:

- ALARMS
- Interrupt Flags: Channel Status
- Interrupt Flags: Channel Monitor

Each section is detailed below.

Alarms

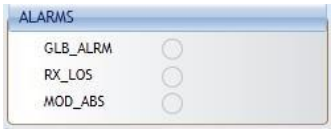


Figure 15: Alarms section

GLB_ALRM, RX_LOS and MOD_ABS are the alarm signals showing the status of the low speed MSA alarm pins.

Interrupt Flags: Channel Status

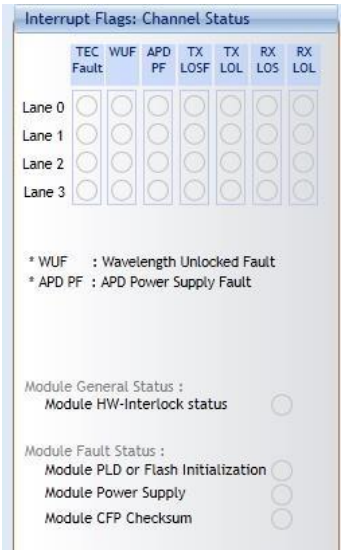


Figure 16: Interrupt Flags: Channel Status section

Network Lane n Fault and Status

A210	**16**	**RO**		**Network Lane n Fault and Status**	**16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.**	**0000h**
			15	Lane TEC Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			14	Lane Wavelength Unlocked Fault	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Lane APD Power Supply Fault	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			12~8	Reserved		0
			7	Lane TX_LOSF	0: Normal; 1: Asserted. (PMD) (FAWS_TYPE_C)	0
			6	Lane TX_LOL	0: Normal; 1: Asserted. (Network) (FAWS_TYPE_B)	0
			5	Reserved		0
			4	Lane RX_LOS	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	Lane RX_LOL	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2~0	Reserved		000b

Figure 17: CFP MSA memory map for Network Lane n Fault and Status registers

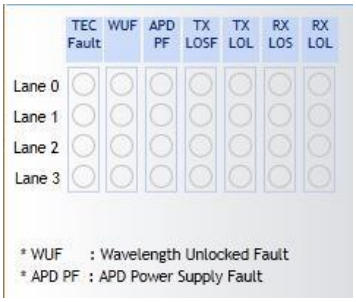


Figure 18: Network Lane n Fault and Status corresponding LEDs

The above figure shows the status LEDs of the flags shown in Figure 17. When a flag is asserted, the corresponding LED is illuminated red.

Module Fault and Status

Module FAWS Registers						
A01D	**1**	**RO**		**Module General Status**		**0000h**
			15	Reserved		0
			14	Reserved		0
			13	HW_Interlock	Module internally generated status signal. (FAWS_TYPE_A) 0: If module power <= Host cooling capacity or if hardware Interlock is not used, 1: If module power > Host cooling capacity.	0
A01E	**1**	**RO**		**Module Fault Status**	**Module Fault Status bit pattern. Only fatal faults that are potentially harmful to the module can trigger the bits here. All the bits are 0: Normal; 1: fault detected. When any bit in this register is a '1', The Module State register will also be set to the Fault State.**	**0000h**
			15~7	Reserved		0
			6	PLD or Flash Initialization Fault	PLD, CPLD, or FPGA initialization fault. (FAWS_TYPE_A)	0
			5	Power Supply Fault	1: Power supply is out of range. (FAWS_TYPE_A)	0
			4~2	Reserved		000b
			1	CFP Checksum Fault	1: CFP Checksum failed. (FAWS_TYPE_A)	0
			0	Reserved		0

Figure 19: CFP MSA Module General Status and FAWS Registers

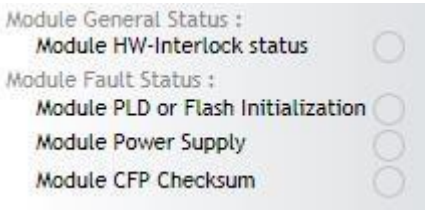


Figure 20: Module General Status and Fault corresponding LEDs

The above window represents the status LEDs of flags shown in Figure 19. When a flag is asserted, the corresponding LED is illuminated red.

Interrupt Flags: Channel Monitor

Alarms and Warnings:

Network Lane Alarms and Warnings

A200	16	RO		Network Lane n Alarm and Warning	16 registers, one for each network lane, represent 16 network lanes. n = 0, 1, …, N-1. N_max = 16. Actual N is module dependent.	0000h
			15	Bias High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			14	Bias High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			13	Bias Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			12	Bias Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			11	TX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			10	TX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			9	TX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			8	TX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_C)	0
			7	Laser Temperature High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			6	Laser Temperature High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			5	Laser Temperature Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			4	Laser Temperature Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			3	RX Power High Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			2	RX Power High Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			1	RX Power Low Warning	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0
			0	RX Power Low Alarm	0: Normal; 1: Asserted. (FAWS_TYPE_B)	0

Figure 21: Network Lane n Alarm and Warning Registers

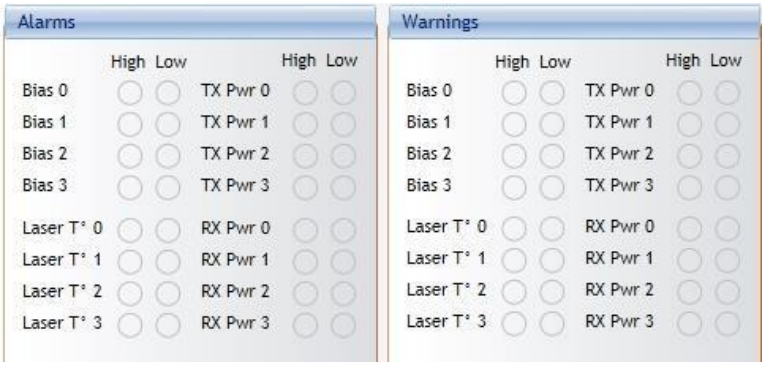


Figure 22: Network Lane n Alarms and Warnings LEDs

The above windows represent the status LEDs of flags shown in fig. 21. There are 4 alarms/warnings that are defined as follows: Laser Bias Current, Laser Temperature, Laser Output Power and Receiver Input Power. When a flag is asserted, the corresponding LED is illuminated red.

Module Alarms and Warnings

A01F	1	RO		Module Alarms and Warnings 1		0000h
			15~12	Reserved		0000b
			11	Mod Temp High Alarm	Mod temp high Alarm. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert.	0
			10	Mod Temp High Warning	Mod temp high Warning. (FAWS_TYPE_A) 0:Normal, 1:Warning assert	0
			9	Mod Temp Low Warning	Mod temp low Warning. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			8	Mod Temp Low Alarm	Mod temp low Alarm. (FAWS_TYPE_A) 0:Normal, 1:Warning assert	0
			7	Mod Vcc High Alarm	Input Vcc high Alarm. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			6	Mod Vcc High Warning	Input Vcc high Warning. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			5	Mod Vcc Low Warning	Input Vcc low Warning. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			4	Mod Vcc Low Alarm	Input Vcc low Alarm. (FAWS_TYPE_A) 0:Normal, 1:Alarm assert	0
			3	Mod SOA Bias High Alarm	SOA bias current high alarm. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0
			2	Mod SOA Bias High Warning	SOA bias current high warning. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0
			1	Mod SOA Bias Low Warning	SOA bias current low warning. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0
			0	Mod SOA Bias Low Alarm	SOA bias current low alarm. (FAWS_TYPE_B) 0:Normal, 1:Alarm assert	0

Figure 23: Module Alarms and Warnings Register

Figure 24: Module Alarms and Warnings LEDs

The above section represents the status LEDs of flags shown in figure 23.

Measurements:

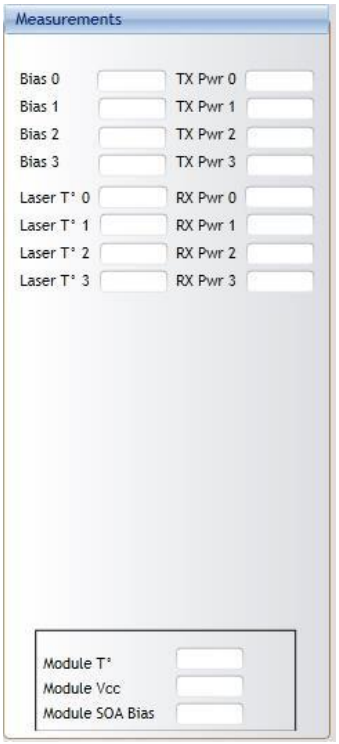


Figure 25: Measurement section

Network Lane n A2D measurements:

Network Lane n Laser Bias Current monitor A2D value: Measured laser bias current, representing a total measurement range of 0 to 131.072 mA.

Network Lane n Laser Output Power monitor A2D value: Measured TX output power, representing a range of laser output power from 0 to 6.5535 mW.

Network Lane n Laser Temp Monitor A2D value: Internally measured temperature in degrees Celsius.

Network Lane n Receiver Input Power monitor A2D value: Measured received input power, representing a power range from 0 to 6.5535 mW.

Module A2D value measurements:

Three analog values, Module Temperature Monitor A/D Value, Module Power Supply 3.3V Monitor A/D Value, and SOA Bias Current A/D Value are measured.

These monitoring values are at the module level and non-network lane specific. The values in these registers are automatically updated by the CFP2 module every 100ms.

7.4.2. Interrupt Masks

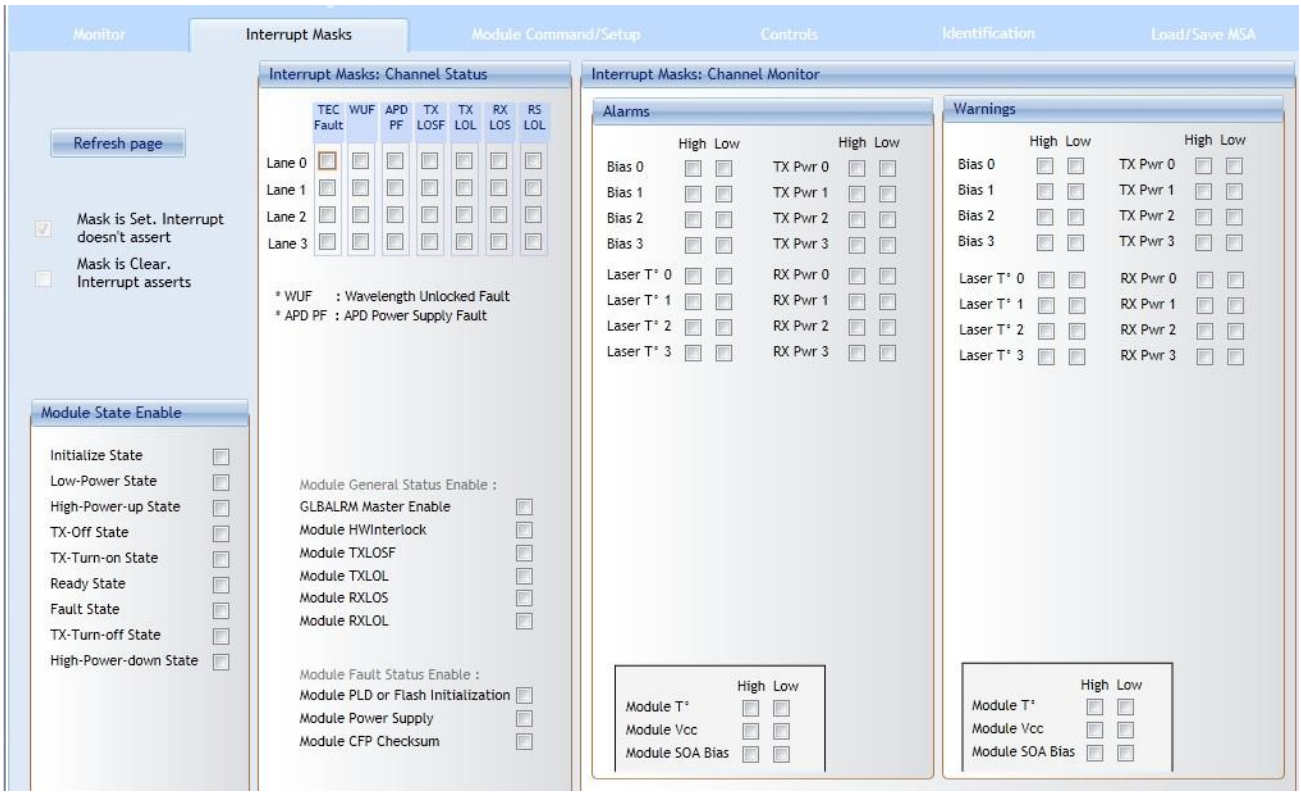


Figure 26: Interrupt Masks tab

All the check boxes provided on this screen either set or clear the corresponding FAWS Enable Registers.

The CFP2 FAWS Enable registers allows the host to enable or disable any particular FAWS bits to contribute to GLB_ALRM. When a mask bit is set, the corresponding alarm or warning will not contribute in triggering the Global Alarm. When a mask is cleared, then the assertion of an alarm or warning will trigger the Global Alarm.

7.4.3. Module Command/Setup

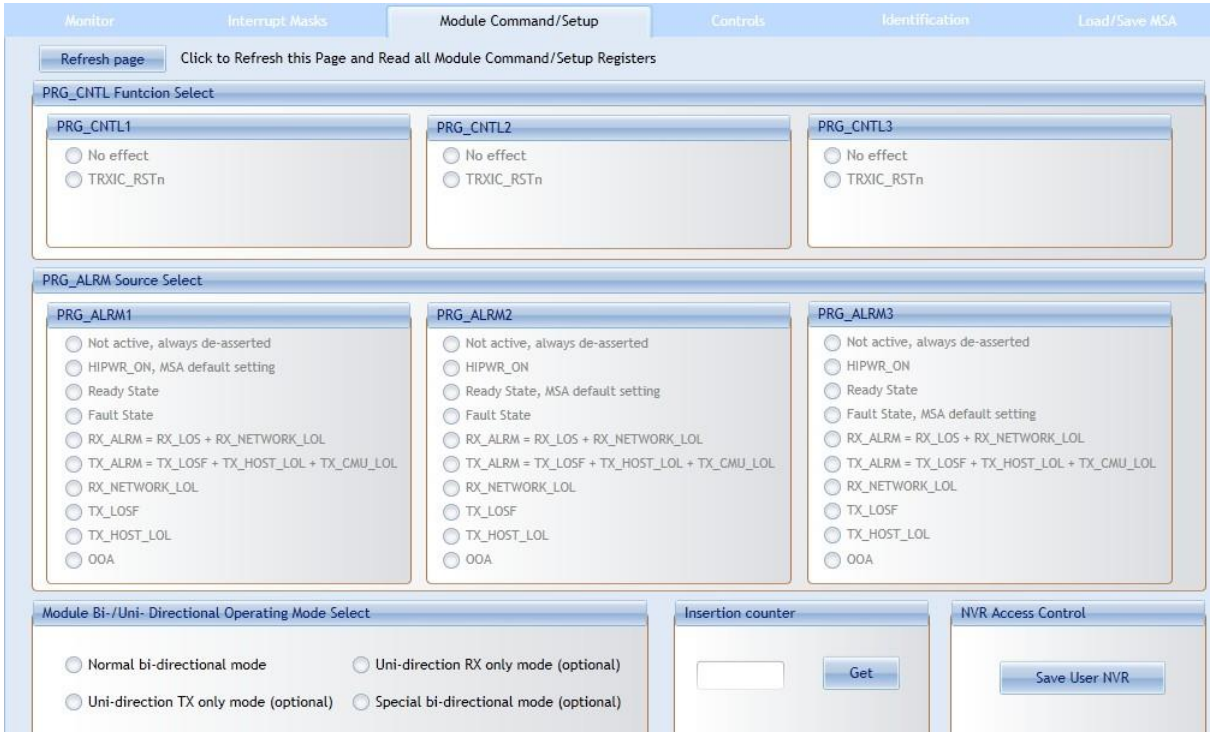


Figure 27: Module Command/Setup screen

This above screen allows customizing some registers that the host uses to control actual module behavior. Through this screen, the user can select a custom control function for the PRG_CNTL hardware pin, or select a custom source for the PRG_ALRM hardware pin alarm, and will also be able to define a module operating mode.

PRG_CNTLs Function Select

A005	1			PRG_CNTL3 Function Select	Selects, and assigns, a control function to PRG_CNTL3.	0000h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_MSB during the Initialize State and it can be programmed to other functions afterward. 0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL3. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL3 Control (A010h.12) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	00h
A006	1			PRG_CNTL2 Function Select	Selects, and assigns, a control function to PRG_CNTL2.	0000h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	This multi-function input is used as HW_IL_LSB during the Initialize State and it can be programmed to other functions afterward. 0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL2. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL2 Control (A010h.11) uses an active high logic, that is, 1 = Assert (Reset). 2~255: Reserved.	00h
A007	1			PRG_CNTL1 Function Select	Selects, and assigns, a control function to PRG_CNTL1.	0001h
		RO	15~8	Reserved		00h
		RW	7~0	Function Select Code	0: No effect, 1: Assign TRXIC_RSTn function to hardware pins PRG_CNTL1. When so assigned this pin uses the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, its soft counterpart Soft PRG_CNTL1 Control (A010h.10) uses an active high logic, that is, 1 = Assert (Reset). TRXIC_RSTn is the CFP MSA default function for PRG_CNTL1. 2~255: Reserved.	01h

Figure 28: CFP MSA PRG_CNTLs Function Select (A005h, A006, A007h) registers

The registers shown in Figure 28 select a control function for the programmable control pins. Each programmable control pin can be programmed with the functions as defined below.

NAME	FUNCTION	VALUE
TRXIC_RSTn	Reset TX and RX ICs, PRG_CNTL1 MSA default.	0: Normal, 1: Assign TRXIC_RSTn function to any of the 3 hardware pins PRG_CNTL3, PRG_CNTL2, and PRG_CNTL1. When so assigned these hardware pins use the active low logic, that is, 0 = Assert (Reset). Note that when so assigned, their soft counterparts Soft PRG_CNTL3, Soft PRG_CNTL2, and Soft PRG_CNTL1 (A010h.12~10) use an active high logic, that is, 1 = Assert (Reset).

Figure 29: Programmable Control Functions

PRG_ALRMs Source Select

A008	1			**PRG_ALRM3 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM3.**	**0003h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, 2: Ready State, 3: Fault State, MSA default setting, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, (Only applicable to certain products. If not implemented in the module, Writing 9 to this register has no effect and shall be read as 0. This is also true for Registers A009h and A00Ah). 10~255: Reserved.	03h
A009	1			**PRG_ALRM2 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM2.**	**0002h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON,	02h
					2: Ready State, MSA default setting, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	
A00A	1			**PRG_ALRM1 Source Select**	**Selects, and assigns, an alarm source for PRG_ALRM1.**	**0001h**
		RO	15~8	Reserved		00h
		RW	7~0	Alarm Source Code	0: Not active, always de-asserted, 1: HIPWR_ON, MSA default setting, 2: Ready State, 3: Fault State, 4: RX_ALRM = RX_LOS + RX_NETWORK_LOL, 5: TX_ALRM = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL, 6: RX_NETWORK_LOL, 7: TX_LOSF, 8: TX_HOST_LOL, 9: OOA, Out of alignment, refer to description of A008h for details, 10~255: Reserved.	01h

Figure 30: CFP MSA PRG_ALRMs Source Select (A008h, A009h, A00Ah) registers

Each of the registers in Figure 30 selects an alarm source for the programmable alarm pins. Each programmable alarm pin can be programmed with the alarm sources defined below.

NAME	ALARM SOURCE	VALUE
HIPWR_ON	Module high-power-on indicator. PRG_ALRM1 MSA default.	0: Module not high powered up, 1: Module high power up completed.
MOD_READY	MOD_READY, module startup sequence done, PRG_ALRM2 MSA default.	0: Not done, 1: Done.
MOD_FAULT	Fault detected. PRG_ALRM3 MSA default.	0: No Fault, 1: Fault.
RX_ALRM	Receive path alarm = RX_LOS + RX_LOL.	0: No receive path alarm, 1: Receive path alarm asserted.
TX_ALRM	Transmit path alarm = TX_LOSF + TX_HOST_LOL + TX_CMU_LOL.	0: No transmit path alarm, 1: Transmit path alarm asserted.
RX_LOL	RX IC Lock Indicator.	0: Locked, 1: Loss of lock.
TX_LOSF	Transmitter Loss of Signal Functionality.	0: All transmitter signals functional, 1: Any transmitter signal not functional
TX_LOL	TX IC Lock Indicator.	0: Locked, 1: Loss of lock.
OOA	Host lane skew out of alignment indicator.	0: No OOA, 1: Out of alignment.

Figure 31: Programmable Alarm Sources

Module Bi-/Uni- directional Operating Mode Select

A00B	**1**			**Module Bi-/Uni-Directional Operating Mode Select**		**0000h**
		RO	15~3	Reserved		0
		RW	2~0	Module Bi/uni-direction mode Select	000b: Normal bi-directional mode, 001b: Uni-direction TX only mode (optional), 010b: Uni-direction RX only mode (optional), 011b: Special bi-directional mode (optional), 100b~111b: Reserved.	000b

Insertion Counter (Multilane CFP4 Modules specific)

This feature is implemented in the ML4050 and ML40501 CFP4 loopback modules; it shows the insertion counter register value.

NVR Access Control

Button Save User NVR will write 0x0020 to register A004 causing the NVR registers to be saved to NVM storage.

7.4.4. Controls

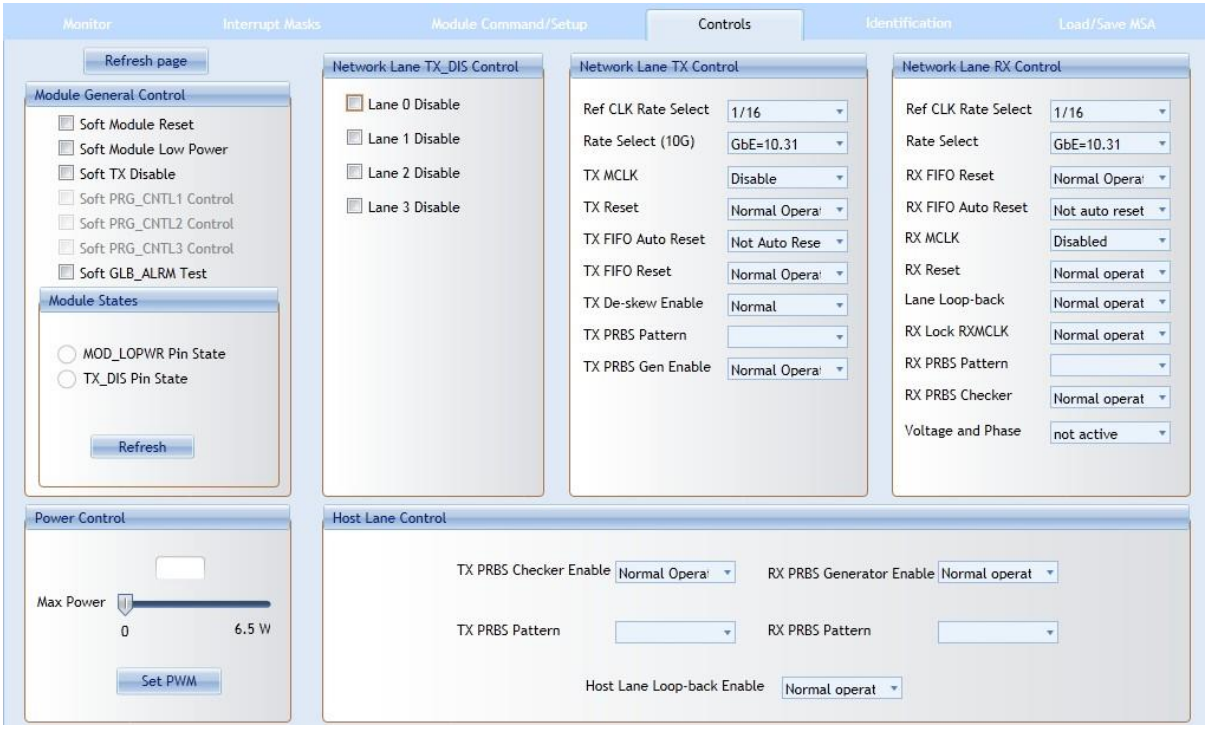


Figure 32: Controls tab

The control screen shown above in Figure 32 provides additional and alternative controls to hardware pins and programmable control pins in controlling the CFP4 module. Please refer to the CFP MSA memory map for an additional description for each control function below.

Module General Control

A010	**1**			**Module General Control**	
		RW/SC	15	Soft Module Reset	Register bit for module reset function. Internally, the bit is OR'ed with MOD_RSTn pin. Host write of 0 has no effect. 1: Module reset asserted.
		RW	14	Soft Module Low Power	Register bit for module low power function. OR'ed with MOD_LOPWR pin. 1: Asserted.
		RW	13	Soft TX Disable	Register bit for TX Disable function. OR'ed with TX_DIS pin. 1: Asserted.
		RW	12	Soft PRG_CNTL3 Control	Register bit for PRG_CNTL3 control function. OR'ed with PRG_CNTL3 pin. 1: Asserted.
		RW	11	Soft PRG_CNTL2 Control	Register bit for PRG_CNTL2 control function. OR'ed with PRG_CNTL2 pin. 1: Asserted.
		RW	10	Soft PRG_CNTL1 Control	Register bit for PRG_CNTL1 control function. OR'ed with PRG_CNTL1 pin. 1: Asserted.
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Asserted
		RO	8~6	Reserved	
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Asserted
		RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Asserted
		RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin. 1: Asserted
		RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin. 1: Asserted
		RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin. 1: Asserted
		RO	0	Reserved	

Figure 33: CFP MSA Module General Control Register A010

Power Control (ML4050 specific)

The user can specify the maximum power consumed by the CFP4 module.

The user should adjust Max Power to the desired value, and then press **Set PWM** to set the maximum allowed values for each thermal spot.

Network Lane n TX_DIS Control

A013	1	RW		Individual Network Lane TX_DIS Control	This register acts upon individual network lanes.
			15	Lane 15 Disable	0: Normal 1: Disable
			14	Lane 14 Disable	0: Normal 1: Disable
			13	Lane 13 Disable	0: Normal 1: Disable
			12	Lane 12 Disable	0: Normal 1: Disable
			11	Lane 11 Disable	0: Normal 1: Disable
			10	Lane 10 Disable	0: Normal 1: Disable
			9	Lane 9 Disable	0: Normal 1: Disable
			8	Lane 8 Disable	0: Normal 1: Disable
			7	Lane 7 Disable	0: Normal 1: Disable
			6	Lane 6 Disable	0: Normal 1: Disable
			5	Lane 5 Disable	0: Normal 1: Disable
			4	Lane 4 Disable	0: Normal 1: Disable
			3	Lane 3 Disable	0: Normal 1: Disable
			2	Lane 2 Disable	0: Normal 1: Disable
			1	Lane 1 Disable	0: Normal 1: Disable
			0	Lane 0 Disable	0: Normal 1: Disable

Figure 34: CFP MSA Individual Network Lane TX_DIS Control Register

Network Lanes TX Control

A011	1			Network Lane TX Control	This control acts upon all the network lanes.	0200h
		RO	15	Reserved		0
		RW	14	TX PRBS Generator Enable	0: Normal operation, 1: PRBS mode. (Optional)	0
		RW	13	TX PRBS Pattern 1	00b:2^7, 01b:2^15, 10b:2^23, 11b:2^31.	00b
		RW	12	TX PRBS Pattern 0		
		RW	11	TX De-skew Enable	0:Normal, 1:Disable	0
		RW	10	TX FIFO Reset	This bit affects both host and network side TX FIFOs. 0: Normal operation, 1: Reset (Optional).	0
		RW	9	TX FIFO Auto Reset	This bit affects both host and network side TX FIFOs. 0: Not Auto Reset, 1: Auto Reset. (Optional).	1
		RW	8	TX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0
		RW	7~5	TX MCLK Control	000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network lane rate, 111b: 1/16 of host lane rate.	000b
		RO	4	Reserved		0b
		RW	3~1	TX Rate Select (10G lane rate)	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b~111b: Reserved.	000b
		RW	0	TX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b

Figure 35: CFP MSA Network Lane TX Control Register

Network Lanes RX Control

A012	1			Network Lane RX Control	This control acts upon all the network lanes.	0200h
		RW	15	Active Decision Voltage and Phase function	This bit activates the active decision voltage and phase function in the module. 0: not active, 1: active. (Optional)	0b
		RW	14	RX PRBS Checker Enable	0: Normal operation, 1: PRBS mode. (Optional)	0b
		RW	13	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31.	00b
		RW	12	RX PRBS Pattern 0		
		RW	11	RX Lock RX_MCLK to Reference CLK	0: Normal operation, 1: Lock RX_MCLK to REFCLK.	0b
		RW	10	Network Lane Loop-back	0: Normal operation, 1: Network lane loop-back. (Optional)	0b
		RW	9	RX FIFO Auto Reset	0: Not auto reset, 1: Auto reset. (Optional).	1b
		RW	8	RX Reset	0: Normal operation, 1: Reset. Definition and implementation are vendor specific.	0b
		RW	7~5	RX MCLK Control	000b: Disabled, 001b: Reserved, 010b: 1/8 of network lane rate, 011b: Reserved, 100b: 1/64 of network lane rate, 101b: 1/64 of host lane rate, 110b: 1/16 of network lane rate, 111b: 1/16 of host lane rate.	000b
		RW	4	RX FIFO Reset	0: Normal, 1: Reset. (Optional).	0b
		RW	3~1	RX Rate Select	000b: GbE=10.31, 001b:SDH=9.95, 010b:OTU3=10.7, 011b:OTU4=11.2, 100b~111b: Reserved.	000b
		RW	0	RX Reference CLK Rate Select	0: 1/16, 1: 1/64.	0b

Figure 36: CFP MSA Network Lane RX Control Register

Host Lane Control

A014	1			Host Lane Control	This control acts upon all the network lanes.
		RO	15	Reserved	
		RW	14	TX PRBS Checker Enable	0:Normal operation, 1:PRBS mode. (Optional)
		RW	13	TX PRBS Pattern 1	00:2^7, 01:2^15, 10:2^23, 11:2^31
		RW	12	TX PRBS Pattern 0	
		RO	11	Reserved	
		RW	10	Host Lane Loop-back Enable	0: Normal operation, 1: Host lane loop-back. (Optional)
		RO	9~8	Reserved	
		RW	7	RX PRBS Generator Enable	0:Normal operation, 1:PRBS mode. (Optional)
		RW	6	RX PRBS Pattern 1	00b: 2^7, 01b: 2^15, 10b: 2^23, 11b: 2^31
		RW	5	RX PRBS Pattern 0	
		RO	4~0	Reserved	

Figure 37: CFP MSA Host Lane Control

7.4.5. Identification

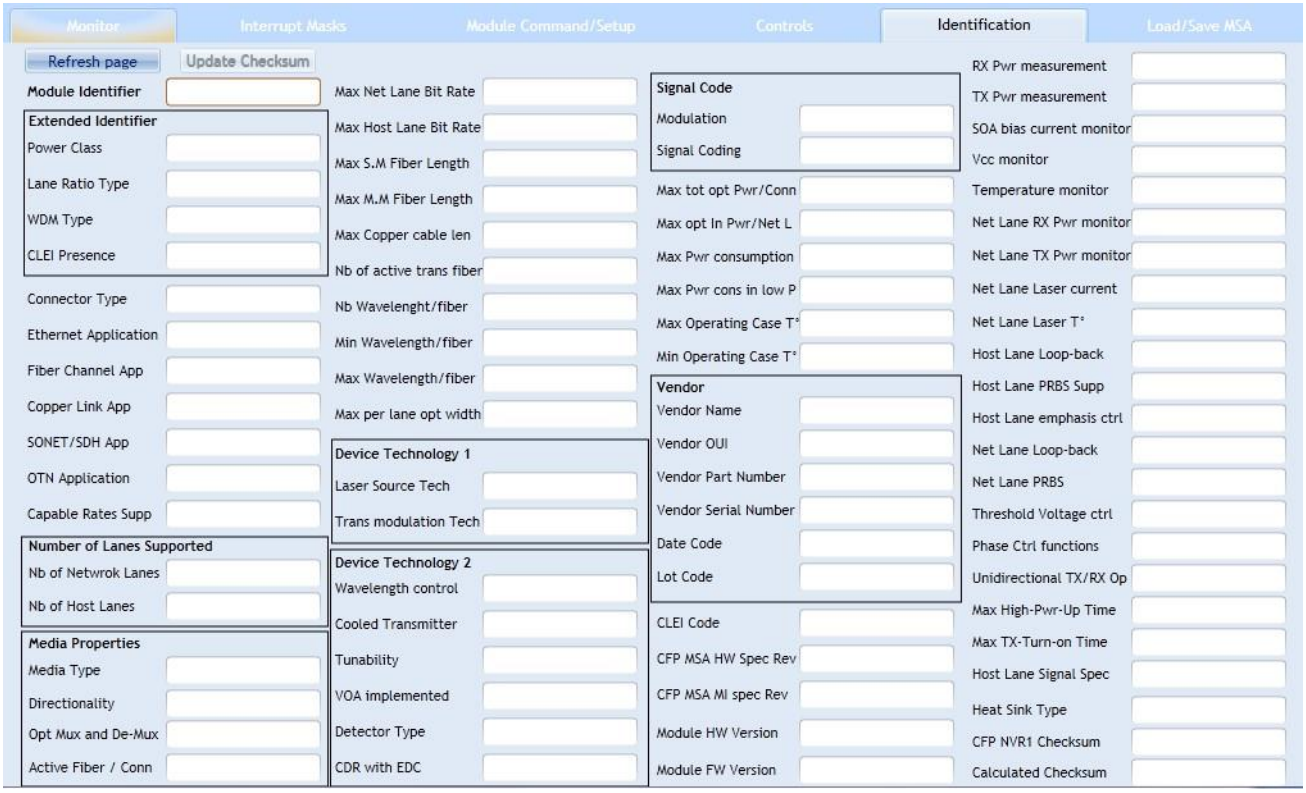


Figure 38: Identification tab

The following sections refers to CFP MSA 2.2 R5 Release, and are presented without any modification or change, the targeted information is read from the correspondent registers, calculated or enumerated when required, and presented to the user on the above screen in a simple readable ASCII format.

Module Identifier (8000h)

For CFP MSA compliant modules, this value shall be 12h. Other module form factors used in the industry are identified with other values. For details, please refer to CFP NVR Table 1.

Extended Identifier (8001h)

It provides additional information about CFP module.

Power Class

As outlined in the CFP MSA Hardware Specification, there are four power classes identified for the CFP MSA. The power classes are provided to allow the host to identify the power requirements of the module and determine if the system is capable of providing and dissipating the specified power class. For a more detailed description, please refer to the CFP MSA Hardware Specification.

Lane Ratio Type

The CFP module shall support network interfaces which may comply with various physical interfaces such as IEEE PMD, SONET/SDH, OTN or that from other standards body. For example, 100GBASE-LR4 network interface corresponds to the optical PMD specified in IEEE clause 88. The CFP module shall also support the Host interface which is instantiated as an electrical interface with multiple lanes operating at a nominal 10Gbps.

WDM Type

It shall identify any optical grid spacing which is in use by the CFP module.

Connector Type Code (8002h)

It shall identify the connector technology used for the network interface. Early iterations of the CFP MSA have identified SC optical connectors, and it is expected that further connectors will be identified.

Ethernet Application Code (8003h)

It shall identify what if any Ethernet PMD application is supported. Any CFP module which supports an application not including Ethernet such as SONET/SDH, OTN, Fiber Channel or other, shall record a 00h to signify that the Ethernet application is undefined. Any CFP module which supports an application which includes Ethernet and additional applications such as SONET/SDH, OTN, Fiber Channel or other, shall record the value in Ethernet Application Code corresponding to the supported Ethernet application.

Fiber Channel Application Code (8004h)

It shall identify what if any Fiber Channel PMD application is supported. Any CFP module which supports an application not including Fiber Channel such as SONET/SDH, OTN, Ethernet or other, shall record a 00h to signify that the Fiber Channel application is undefined. Any CFP module which supports an application which includes Fiber Channel and additional applications such as SONET/SDH, OTN, Ethernet

or other, shall record the value in Fiber Channel Application Code corresponding to the supported Fiber Channel application.

Copper Link Application Code (8005h)

In this CFP register, the CFP module shall identify what if any non-Ethernet Copper based PMD application which is supported. At the time of the writing, this application is undefined.

SONET/SDH Application Code (8006h)

It shall identify what if any SONET/SDH PMD application is supported. Any CFP module which supports an application not including SONET/SDH such as Ethernet, OTN, Fiber Channel or other, shall record a 00h to signify that the SONET/SDH application is undefined. Any CFP module which supports an application which includes SONET/SDH and additional applications such as Ethernet, OTN, Fiber Channel or other, shall record the value in SONET/SDH Application Code corresponding to the supported SONET/SDH application.

OTN Application Code (8007h)

It shall identify what if any OTN PMD application is supported. Any CFP module which supports an application not including OTN such as SONET/SDH, Ethernet, Fiber Channel or other, shall record a 00h to signify that the OTN application is undefined. Any CFP module which supports an application which includes OTN and additional applications such as SONET/SDH, Ethernet, Fiber Channel or other, shall record the value in OTN Application Code corresponding to the supported OTN application.

Additional Capable Rates Supported (8008h)

Number of Lanes Supported (8009h)

The network lane number assignment shall always start from 0h and end with the number of lanes supported minus one, with no number skipped in between. This shall be applicable to both network and host lanes whether the lane numbers are different or the same. For example, a serial network lane implementation shall use lane 0 and a 4 network lane PMD shall use lane number 0 ~ 3. A CAUI host interface shall use lane numbers 0 ~ 9.

Number of Network Lanes

It is a 4-bit number representing the number of network data I/O supported in this module. The value of 0 represents 16 network data I/O supported. The values of 1 through 15 represent the actual number of network lanes supported.

Number of Host Lanes

It is a 4-bit number representing the number of host data I/O supported in this module. The value of 0 represents 16 host data I/O supported. The values of 1 through 15 represent the actual number of host lanes supported.

Media Properties (800Ah)

Media Type

It shall identify the type of transmission media for the supported application using bits 7~6.

Directionality

It shall identify if supported application uses the same transmission media for the transmit/receive network interfaces (Bi-Directional) or if separate transmission media are required for transmit and receive network interfaces, respectively.

Optical Multiplexing and De-Multiplexing

It shall identify if optical multiplexing and optical de-multiplexing are supported within the CFP module.

Active Fiber per Connector

It shall identify the number of active TX/RX fiber pairs in an optical connector. For example, a CFP module supporting the 100GBASE-SR10 application using an MPO connector shall report 10 in Active Fiber per Connector.

Maximum Network Lane Bit Rate (800Bh)

It shall identify maximum data rate supported per network lane. For more complex modulation schemes than OOK (on/off keying), the value reported shall be the bit rate and not the baud rate. The value shall be based upon units of 0.2 Gbps. A value of 0h is considered undefined.

Maximum Host Lane Bit Rate (800Ch)

It shall identify maximum data rate supported per host lane. The value shall be based upon units of 0.2 Gbps. The nominal lane rate suggested in the CFP MSA HW Specification is 10Gbps. However, various applications such as support for OTU4 and future applications will require higher lane rates. A value 0h is considered undefined.

Maximum Single Mode Optical Fiber Length (800Dh)

It shall identify the specified maximum reach supported by the application for transmission over single mode fiber. The value shall be based upon units of 1km. For applications which operate over compensated transmission systems, it is suggested to enter an undefined value. A value of 0h is considered undefined.

Maximum Multi-Mode Optical Fiber Length (800Eh)

It shall identify the specified maximum reach supported by the application for transmission over OM3 multi-mode fiber. The value shall be based upon units of 10 m. A value of 0h is considered undefined.

Maximum Copper Cable Length (800Fh)

The module shall identify the specified maximum reach supported by the application for transmission over copper cable. The value shall be based upon units of 1 m. A value of 0h is considered undefined.

Number of Active Transmit Fibers

Bits 4~0 are a value identifying the number of active optical fiber outputs supported. The value 0 represents 0 active transmit fibers (i. e., receive-only), copper or undefined. The values of 1 through 31 represent the actual number of active transmit fibers. For example, the value for 100GBASE-SR10 is 10.

Number of Wavelengths per Active Transmit Fiber

Bits 4~0 are a value representing the number of wavelengths per active transmit fiber. The value 0h represents an 850 nm multimode source or undefined. The values 1 through 31 represent the actual number of wavelengths per transmit fiber. For example, the value for 100GBASE-LR4 is 4.

Minimum Wavelength per Active Fiber (8012h, 8013h)

It is a 16-bit unsigned value data field and shall identify the minimum wavelength, in the unit of 25 pm, of any supported optical fiber output per the application. For an example, the value for 100GBASE-LR4 with a minimum specified wavelength of 1294.53 nm would be CA45h. A value of 0 indicates a multimode source or undefined.

Maximum Wavelength per Active Fiber (8014h, 8015h)

It is a 16-bit unsigned value data field and shall identify the maximum wavelength, in the unit of 25 pm, of any supported optical fiber output per the application. For an example, the value for 100GBASE-LR4 with a maximum specified wavelength of 1310.19 nm would be CCB8h. A value of 0 indicates a multimode source or undefined.

Maximum per Lane Optical Width (8016h, 8017h)

It shall identify the maximum network lane optical wavelength width, in the unit of 1pm, of any supported optical fiber output per the application. For an example, the value for

100GBASE-LR4 with a maximum specified optical wavelength width of 2.1nm for network lane L3 would be 834h. A value of 0 indicates a multimode source or undefined.

Device Technology 1 (8018h)

Laser Source Technology

It shall identify the type of laser technology which is used. There is a CFP register value for electrical/copper (non-laser) transmission, as well as additional reserved space for as of yet undefined laser types.

Transmitter Modulation Technology

It shall identify the type of modulation technology used. This is a 4-bit unsigned value representing commonly used modulation technologies with reserved values to represent for as of yet undefined modulator types.

Device Technology 2 (8019h)

Several data fields in this register are related to tunable transmitters. However the full support of tunability is not fully covered in the Draft. It shall be supported either in the future release of this draft or in a follow-up MSA.

Wavelength Control

It shall identify if the wavelength of the laser technology which is used includes an active wavelength control mechanism. Active wavelength control mechanism is defined to be a wavelength sensitive device which can be used to compare the actual transmitted wavelength from the expected transmitted wavelength. The value of 0b signifies no control mechanism and 1b signifies the presence of such a mechanism within the CFP module.

Cooled Transmitter

It shall identify if the transmitter is coupled to a cooling mechanism within the module. A popular implementation for such a coupled cooling mechanism is to mount a laser such that it is thermally coupled to a thermoelectric cooler which is controlled to keep the laser within a defined temperature range. If any cooling mechanism is present the transmitter is considered to be cooled. A transmitter is considered to be cooled even if the cooling mechanism is not always active. The value of 0b signifies no cooling mechanism and 1b signifies the presence of such a cooling mechanism within the CFP module.

Tunability

It shall identify if the transmitted optical wavelength may be tuned over a specified spectral range. The value of 0b signifies no tuning mechanism and 1b signifies the presence of such a tuning mechanism within the CFP module.

VOA Implemented

It shall identify if the optical receiver implements a variable optical attenuator (VOA) within the optical receive chain. The value of 0b signifies no VOA mechanism and 1b signifies the presence of such a VOA mechanism within the CFP module.

Detector Type

It shall identify the type of detector technology which is used. There is a CFP register value for undefined detector types.

CDR with EDC

It shall identify if the Clock and Data Recovery (CDR) circuitry within the CFP module receive path contains any electronic dispersion compensation (EDC) techniques to improve the receiver performance.

It is recognized that there exist a variety of EDC techniques with varying performance enhancements and tradeoffs – this CFP register does not convey any detail, only if the CFP module implements EDC within the receiver. The value of 0b signifies no EDC mechanism and "1" signifies the presence of such an EDC mechanism within the CFP module.

Signal Code (801Ah)

Modulation

It shall identify the polarity coding used in the optical modulation. A value of 0b is considered undefined.

Signal Coding

It shall identify the signaling coding used in the optical modulation. A value of 0b is considered undefined.

Maximum Total Optical Output Power per Connector (801Bh)

It shall identify the maximum optical output power of any supported optical fiber output per the application. A value of 0h is considered undefined.

Maximum Optical Input Power per Network Lane (801Ch)

It shall identify the maximum optical input power of any supported optical fiber input per the application. A value of 0h is considered undefined.

Maximum Power Consumption (801Dh)

It shall identify the maximum power consumption of any supported application. A value of 0h is considered undefined.

Maximum Power Consumption in Low Power Mode (801Eh)

It shall identify the maximum power consumption of the low power mode state. The low power mode state is described in detail in the CFP MSA Hardware specification. A value of 0h is considered undefined.

Maximum Operating Case Temp Range (801Fh)

It shall identify the maximum operating case temperature specified of any supported application. It is a signed 8-bit value expressed in two's-complement, representing a total range from -127 to +127 in increments of 1 degree C'. The value -128 (80h) indicates the value is not defined.

Minimum Operating Case Temp Range (8020h)

It shall identify the minimum operating case temperature specified of any supported application. It is a signed 8-bit value expressed in two's-complement, representing a total range from -127 to +127 in increments of 1 degree C'. The value -128 (80h) indicates the value is not defined.

Vendor Name (8021h)

It shall identify the CFP module Vendor name in ASCII code. The vendor name is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name or the stock exchange code for the corporation. Vendor is the CFP module vendor.

Vendor OUI (8031h)

It is a 3 byte field that contains the IEEE Company Identifier for CFP module vendor (as opposed to the OUI of any third party ICs which may be used therein). Bit order for the OUI follows the format of IEEE 802.3 Clause 22.2.4.3.1 and is therefore reversed in comparison to other NVRs. A value of all zero in the 3 byte field indicates that the Vendor OUI is unspecified. Vendor is the CFP module vendor.

Vendor Part Number (8034h)

It is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16 byte field indicates that the Vendor Part Number is unspecified. Vendor is the CFP module vendor.

Vendor Serial Number (8044h)

It is a 16 byte field that contains ASCII characters, left aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number. A value of all zero in the 16 byte field indicates that the Vendor SN is unspecified. Vendor is the CFP module vendor.

Date Code (8054h)

It is an 8 byte field that contains the vendor's date code in ASCII characters. A value of all zero in the 8 byte field indicates that the Vendor date code is unspecified. Vendor is the CFP module vendor.

Lot Code (805Ch)

It is a 2-byte field that contains the vendor's lot code in ASCII characters. A value of all zero in the 2-byte field indicates that the Vendor lot code is unspecified. Vendor is the CFP module vendor.

CLEI Code (805Eh)

It is a 10 byte field that contains the Common Language Equipment Identifier code in ASCII characters. A value of all zero in the 10 byte field indicates that the CLEI code is unspecified.

CFP MSA Hardware Specification Revision Number (8068h)

It indicates the CFP MSA hardware specification version number supported by the transceiver. This 8-bit value represents the version number times 10. This yields a max of 25.5 revisions.

CFP MSA Management Interface Specification Revision Number (8069h)

It indicates the CFP MSA Management specification version number supported by the CFP module. This 8-bit value represents the version number times 10. This yields a max of 25.5 revisions.

Module Hardware Version Number (806Ah)

It is a 2-byte number in the format of x.y with x at lower address and y at higher address. In each register this 8-bit value represents the version number from 0 to 255. A value of all zero in this 2-byte field indicates that the vendor HW version number is unspecified.

Module Firmware Version Number (806Ch)

It is a 2-byte field in the format of “x.y”. The “x” value is contained within the lower address. The “y” value is contained in the upper address. In each register this 8-bit value represents the release number from 0 to 255. A value of all zero in this 2-byte field indicates that the vendor FW version number is unspecified.

Digital Diagnostic Monitoring Type (806Eh)

It is a one byte field with 8 single bit indicators describing how DDM functions are implemented in CFP module.

Digital Diagnostic Monitoring Capability 1 (806Fh)

It describes DDM functions implemented at CFP module level (not lane specific). This

MSA draft specifies 4 A/D inputs, transceiver SOA bias current monitor, transceiver power supply voltage monitor, transceiver internal temperature monitor, and transceiver case temperature monitor. The last quantity, transceiver case temperature monitor is intended for supplying an additional monitor to transceiver internal temperature monitor. The definition and implementation of case temperature is left to be specified by vendor datasheet.

Digital Diagnostic Monitoring Capability 2 (8070h)

It describes DDM functions implemented at network lane level.

Module Enhanced Options (8071h)

It describes enhanced optional functions implemented in CFP module. Refer to register description for details.

Maximum High-Power-up Time (8072h)

It is for a vendor defined parameter which specifies the maximum time to transit the "High- Power-up" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value * 1 second. Use 1 second if the actual time is less than one second.

Maximum TX-Turn-on Time (8073h)

It is for a vendor defined parameter which specifies the maximum time to transit the "TX Turn-on" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*.

The Host may use this value as the time-out value. It is an unsigned 8-bit value in units of 1 second. Use 1 second if the actual time is less than 1 second.

Host Lane Signal Spec (8074h)

It specifies the host lane signal type a module supports. Refer to register description for details.

Heat Sink Type (8075h)

It identifies if the top surface of the CFP module has a flat top or integrated heat sink. The CFP MSA supports various networking applications which may require different thermal management solutions. The default top surface of the CFP module is a flat top, however, some networking applications will benefit from an integrated heat sink. An integrated heat sink complies with the total module height requirements and shall not disrupt, disable nor damage any riding heat sink system. For further details, refer to the CFP MSA Hardware specification.

Maximum TX-Turn-off Time (8076h)

It is for a vendor defined parameter which specifies the maximum time to transit the "TX Turn-off" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*.

The Host may use this value as the time-out value. It is an unsigned 8-bit value in units of ms. Use 1 ms if the actual time is less than 1 second.

Maximum High-Power-down Time (8077h)

It is for a vendor defined parameter which specifies the maximum time to transit the "High- Power-down" state shown in *Figure 3 State Transition Diagram during Startup and Turn-off*. The Host may use this value as the time-out value. It is an unsigned 8-bit value * 1 second. Use 1 second if the actual time is less than one second.

Module Enhanced Options 2 (8078h)

It describes the second enhanced optional functions implemented in CFP module. Refer to register description for details.

Transmitter Monitor Clock Options (8079h)

This register contains the transmitter monitor clock option bits. The clock is intended to be used as a reference for measurements of the optical output. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data.

Receiver Monitor Clock Options (807Ah)

This register contains the receiver monitor clock option bits. The clock is intended to be used as a reference for measurements of the optical input. If provided, the clock shall operate at a rate relative to the optical lane rate of 1/16 rate for 40Gbit/s applications and a 1/8 rate of 25Gbit/s for 100Gbit/s applications. Another option is a clock at 1/16 or 1/64 the rate of transmitter electrical input data.

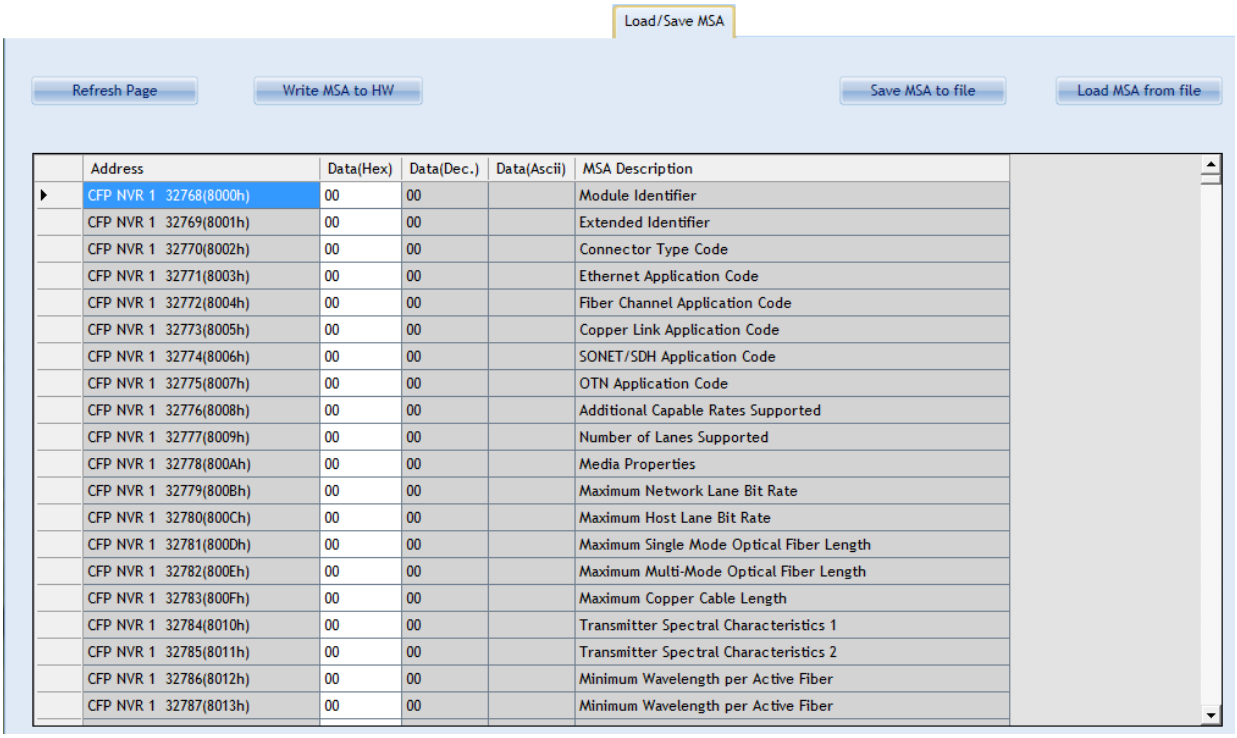
Module Enhanced Options 3 (807Bh)

It describes the third enhanced optional functions implemented in CFP module. Refer to register description for details.

CFP NVR 1 Checksum (807Fh)

It is the 8 bit unsigned result of the checksum of all of the CFP register LSB contents from addresses 8000h to 807Eh inclusive. Note that all the reserved registers have zero value contribution to the calculation of this Checksum.

7.4.6. Load/Save MSA



Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description
CFP NVR 1 32768(8000h)	00	00		Module Identifier
CFP NVR 1 32769(8001h)	00	00		Extended Identifier
CFP NVR 1 32770(8002h)	00	00		Connector Type Code
CFP NVR 1 32771(8003h)	00	00		Ethernet Application Code
CFP NVR 1 32772(8004h)	00	00		Fiber Channel Application Code
CFP NVR 1 32773(8005h)	00	00		Copper Link Application Code
CFP NVR 1 32774(8006h)	00	00		SONET/SDH Application Code
CFP NVR 1 32775(8007h)	00	00		OTN Application Code
CFP NVR 1 32776(8008h)	00	00		Additional Capable Rates Supported
CFP NVR 1 32777(8009h)	00	00		Number of Lanes Supported
CFP NVR 1 32778(800Ah)	00	00		Media Properties
CFP NVR 1 32779(800Bh)	00	00		Maximum Network Lane Bit Rate
CFP NVR 1 32780(800Ch)	00	00		Maximum Host Lane Bit Rate
CFP NVR 1 32781(800Dh)	00	00		Maximum Single Mode Optical Fiber Length
CFP NVR 1 32782(800Eh)	00	00		Maximum Multi-Mode Optical Fiber Length
CFP NVR 1 32783(800Fh)	00	00		Maximum Copper Cable Length
CFP NVR 1 32784(8010h)	00	00		Transmitter Spectral Characteristics 1
CFP NVR 1 32785(8011h)	00	00		Transmitter Spectral Characteristics 2
CFP NVR 1 32786(8012h)	00	00		Minimum Wavelength per Active Fiber
CFP NVR 1 32787(8013h)	00	00		Minimum Wavelength per Active Fiber

Figure 39: Load/Save MSA tab

This tab allows user to Load or Save his custom CFP4 configuration.

Once data is gathered, it will be displayed in a grid showing: register address, hex value, ASCII value, register description.

- **Refresh Page button:** Read CFP MSA Registers, and refresh values.
- **Write MSA to HW button:** Write the current MSA configuration to CFP4 module.
- **Save MSA to file button:** saves the current MSA memory to a file using CSV (comma separated values) format.
- **Load MSA from file button:** Loads MSA values from file and map it to MSA memory.

1.1.1 Threshold Registers

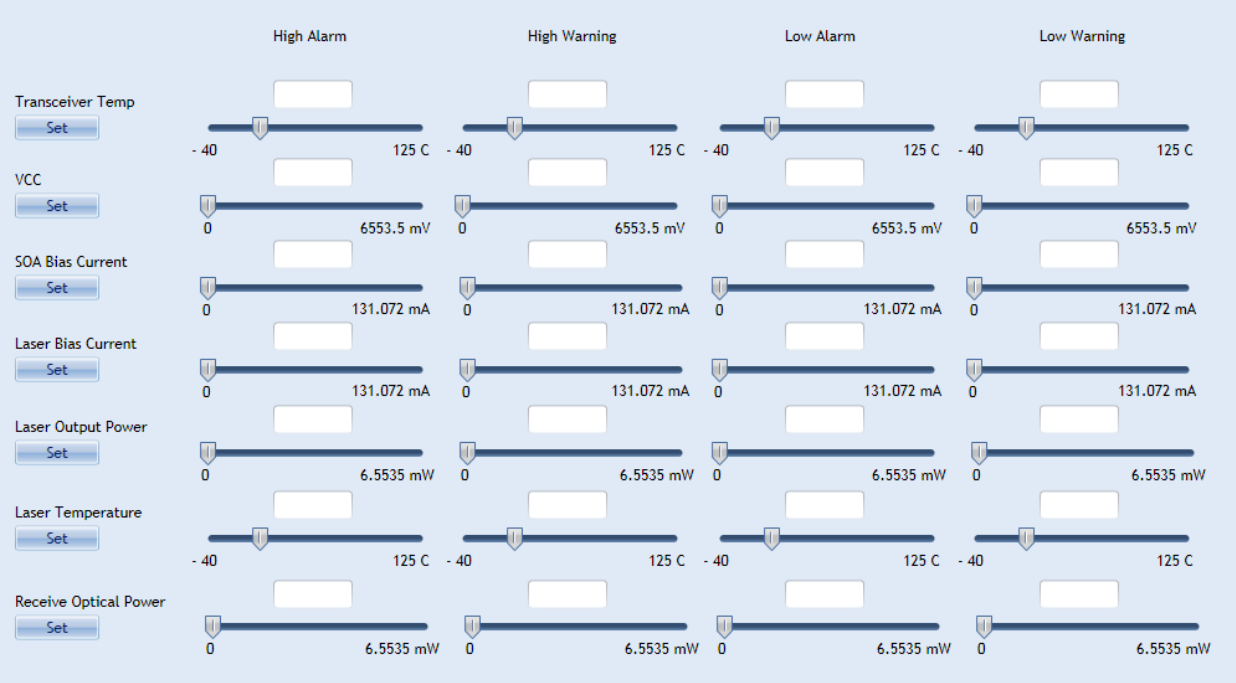


Figure 40: Threshold registers tab

This tab allows the user to update the values of the alarm and warning threshold registers. The minimum and maximum scope of the values is as specified by CFP MSA.

Each A/D value has a corresponding high alarm, low alarm, high warning and low warning threshold.

The figure below shows the MSA memory map for the above values.

CFP NVR 2						
Hex	***Size***	***Access***	***Bit***	***Register Name***	***Description***	***LSB Unit***
Alarm/Warning Threshold Registers						
8080	**2**	**RO**	**7~0**	**Transceiver Temp High Alarm**	**These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127 255/256 degree C. MSA valid range is between –40 and +125C." MSB stored at low address, LSB stored at high address.**	**1/256 degC**
8082	**2**	**RO**	**7~0**	**Transceiver Temp High Warning**		
8084	**2**	**RO**	**7~0**	**Transceiver Temp Low Warning**		
8086	**2**	**RO**	**7~0**	**Transceiver Temp Low Alarm**		
8088	**2**	**RO**	**7~0**	**VCC High Alarm Threshold**	**These thresholds are an unsigned 16-**	**0.1**
808A	**2**	**RO**	**7~0**	**VCC High Warning Threshold**	**bit integer with LSB = 0.1 mV, representing a range of voltage from 0**	**mV**
808C	**2**	**RO**	**7~0**	**VCC Low Warning Threshold**		
808E	**2**	**RO**	**7~0**	**VCC Low Alarm Threshold**		
8090	**2**	**RO**	**7~0**	**SOA Bias Current High Alarm**	**These threshold values are an**	**2 uA**

8092	2	RO	7~0	SOA Bias Current High Warning	unsigned 16-bit integer with LSB = 2 uA, representing a range of current from 0 to 131.072 mA. MSB stored at low address, LSB stored at high address.	
8094	2	RO	7~0	SOA Bias Current Low Warning		
8096	2	RO	7~0	SOA Bias Current Low Alarm		
8098	2	RO	7~0	Auxiliary 1 Monitor High Alarm Threshold	TBD	TBD
809A	2	RO	7~0	Auxiliary 1 Monitor High Warning	TBD	
809C	2	RO	7~0	Auxiliary 1 Monitor Low Warning	TBD	
809E	2	RO	7~0	Auxiliary 1 Monitor Low Alarm	TBD	
80A0	2	RO	7~0	Auxiliary 2 Monitor High Alarm Threshold	TBD	TBD
80A2	2	RO	7~0	Auxiliary 2 Monitor High Warning	TBD	
80A4	2	RO	7~0	Auxiliary 2 Monitor Low Warning	TBD	
80A6	2	RO	7~0	Auxiliary 2 Monitor Low Alarm	TBD	
80A8	2	RO	7~0	Laser Bias Current High Alarm	Alarm and warning thresholds for measured laser bias current. Reference A2A0h Description for additional information. MSB stored at low address, LSB stored at high address.	See A2A0h
80AA	2	RO	7~0	Laser Bias Current High Warning		
80AC	2	RO	7~0	Laser Bias Current Low Warning		
80AE	2	RO	7~0	Laser Bias Current Low Alarm		
80B0	2	RO	7~0	Laser Output Power High Alarm	Alarm and warning thresholds for measured laser output power. Reference A2B0h Description for	See A2B0h
80B2	2	RO	7~0	Laser Output Power High Warning		
80B4	2	RO	7~0	Laser Output Power Low Warning	low address, LSB stored at high address.	
80B6	2	RO	7~0	Laser Output Power Low Alarm		
80B8	2	RO	7~0	Laser Temperature High Alarm	Alarm and warning thresholds for measured received input power. Reference A2C0h Description for additional information. MSB stored at low address, LSB stored at high	See A2C0h
80BA	2	RO	7~0	Laser Temperature High Warning		
80BC	2	RO	7~0	Laser Temperature Low Warning		
80BE	2	RO	7~0	Laser Temperature Low Alarm		
80C0	2	RO	7~0	Receive Optical Power High Alarm	Alarm and warning thresholds for measured received input power. Reference A2D0h Description for additional information. MSB stored at low address, LSB stored at high address.	See A2D0h
80C2	2	RO	7~0	Receive Optical Power High Warning		
80C4	2	RO	7~0	Receive Optical Power Low Warning		
80C6	2	RO	7~0	Receive Optical Power Low Alarm		
80C8	55	RO	7~0	Reserved		0

80FF	1	RO	7~0	CFP NVR 2 Checksum	The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h	NA

Figure 41: Threshold Registers MSA memory map

7.4.7. CFP Module Vendor I/O pins

These pins can be controlled by the external pin header J18 on the Host Board, or from the GUI.

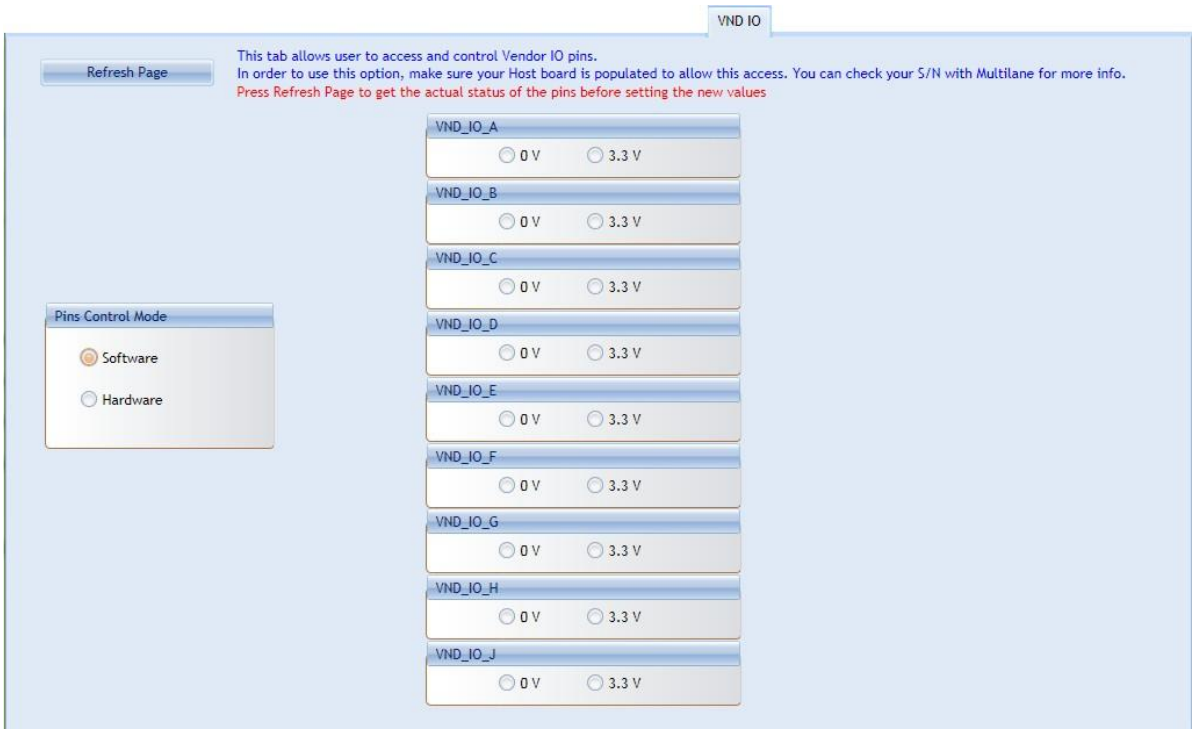


Figure 42: VND IO Tab

This is the VND IO tab which provides control access to CFP2 Module Vendor I/O pins.

In Pins Control Mode:

- Select Software option to gain Software control for VND_IO pins, and drive them from the host microcontroller
- Select Hardware option to release the pins from microcontroller and control them from pin header male J18 on the Host by either applying 3.3V or 0V from an external source.

Software Mode:

The **Refresh Page** button will read the current pins status and update the GUI values accordingly, thus user can check the current state of all VND_IO pins at any time by pressing the refresh button.

Each VND_IO pin can be controlled from its corresponding GroupBox, allowing user to set any pin independently to 0V or 3.3V.

1.1.2 DVT tab

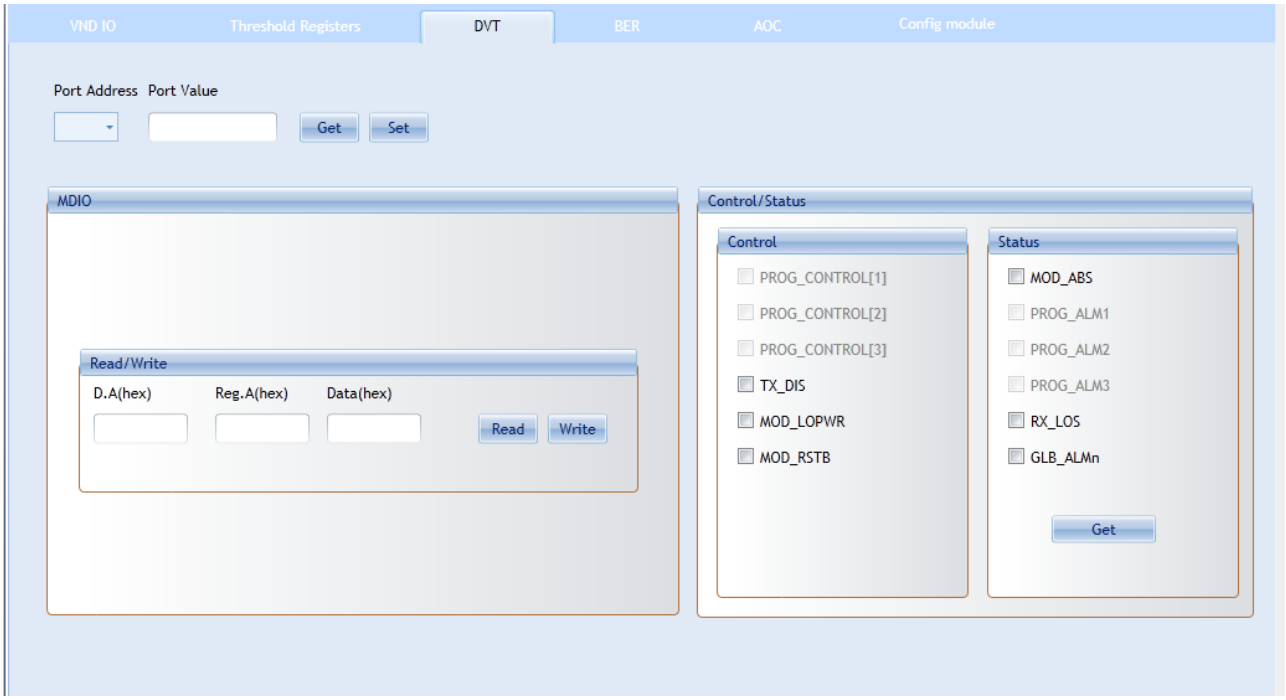


Figure 43: DVT tab

This tab allows user to directly control the ML4049 Micro.

- One can choose a specific Port Address on the Micro and Get or Set its value (in Hex).
- Read/Write MDIO from a specific Device Address and Register Address.
- Change the control pins level.
- Get the Status pins values.

1.1.3 Changing Port Address

When the module is initialized, the default port address is automatically set to 0.

However the user will be able to change the Port Address anytime by entering the new Hexadecimal value in the **Port Address (hex)** textbox shown in Figure 43 below and Press the **Set** button.

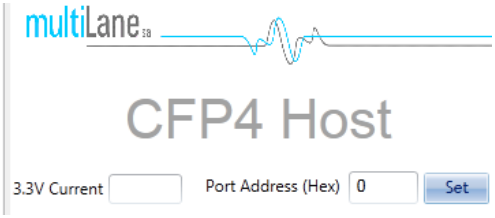


Figure 44: GUI header

8. API

An API file containing all the ML4049 functions can be provided; these functions allow access to the alarm and control signals as well as to the MDIO Master commands. Hence, users can implement these functions according to their own requests and using the platform that responds to their requirements.

Revision History

Revision	Description	Date
0.1	▪ Preliminary revision	29/08/2016