ML4030-DCO

Technical Reference

CFP2-DCO Electrical Passive Loopback Modules

MSA Compliant 200G/400G

Innovation for the next generation

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1 Overview

The **ML4030-DCO** is a CFP2 passive electrical loopback module with a hot pluggable form factor designed for CFP2 host ports high speed testing applications. The **ML4030-DCO** is designed for 200/400 Gigabit Ethernet applications and provides 8x56G RX and TX lanes, a MDIO module management interface and all the CFP2 MSA hardware signals.
The **ML4030-DCO** loops 8-lane up to 56 Gb/s transmit data from the Host back to 8-lane up to 56 GB/s receive data to the Host.
The **ML4030-DCO** provides programmable power dissipation up to 36 W allowing the module to emulate all the CFP2-DCO power classes.

1.1 ML4030-DCO 8x56G Passive Loopback Module | Key Features

- Passive CFP2-DCO loopback module, 8 TX & 8 RX Lanes operating up to 56 Gb/s per lane
- Programmable Power Dissipation up to 36 W covering all CFP2-DCO power classes
- Custom Memory Maps
- RX_LOS-Alarm driven by TX_DIS control
- High performance Signal Integrity traces
- MSA compliant Digital Diagnostic and Monitoring Interface (DDMI)
- 3 Status LED indicator
- Built with advanced PCB material
- Temperature sensing
- Cut-Off Temperature preventing module overheating
- Hot Pluggable module

1.2 LED Indicator

Green (Solid) – Module is in high power mode.
Red (Solid) – Module is in low power mode.
Green/Red (Blinking) – Module is overheated and the temperature high alarm is asserted

1.3 Recommended Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		0		85	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.6	V
Data Rate	Rb	Guaranteed to work up to 56 Gbps per lane	0		200/400	Gbps

Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0		36	W

2 Functional Description

2.1 Management Data Interface – MDIO

The **ML4030-DCO** supports the MDIO interface specified in IEEE802.3 Clause 45.
The **ML4030-DCO** implements a dedicated MDIO logic block to handle the high rate MDIO data and a CFP register space that is divided into two register groups, the Non-Volatile Registers (NVR) and the Volatile Registers (VR). The NVRs are connected to a Non-Volatile Memory device (NVM) for ID/Configuration data storage. Over the internal bus system, the VRs are connected to a device that executes the Host control commands and reports various Digital Diagnostic Monitoring (DDM) data. Please Note that in the rest of this document, independently of implementation, CFP registers are also referred to as NVRs or VRs.

The **ML4030-DCO** specifications are the following:

- Supports MDC rates up to 4 MHz.
- CFP Registers at MDIO Device Address 1 as specified by CFP MSA.
- Supports various Physical Addresses thus allowing communication with many modules plugged to the same Host with different Port Addresses (PRT_ADDR0-2) assigned.

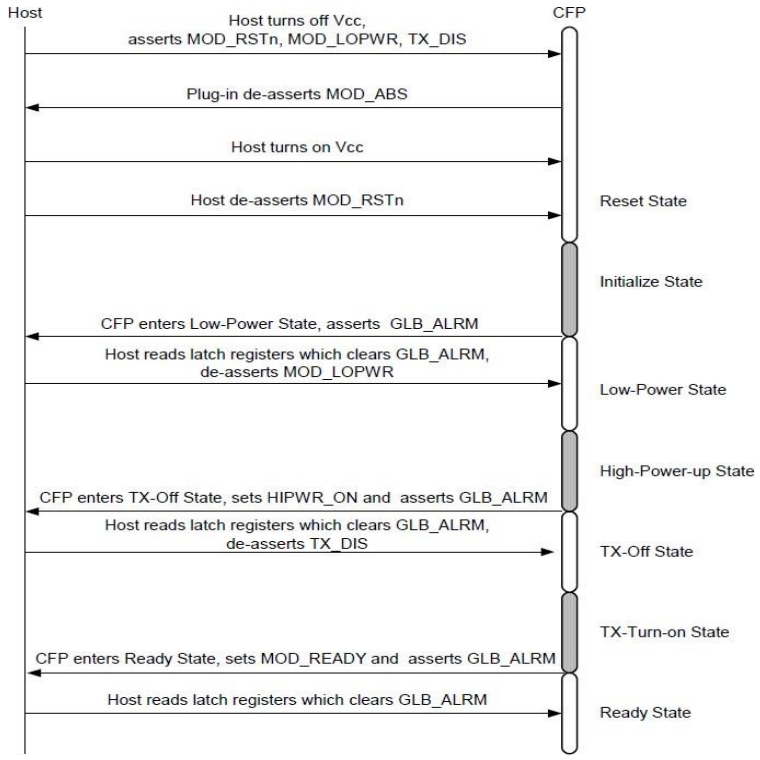
CFP registers use fast memory to shadow the NVM data and the DDM data. The shadow registers decouple the Host-side timing requirements from the module's internal processing, timing, and hardware control circuit introduced latency.
CFP shadow register set meets the following requirements:

- It supports dual access from the Host and from module internal operations such as NVM and DDM data transfers.
- It supports continuous Host access (read and write) with fast access memory at maximum MDC rates of 4 MHz.
- It allows the uploading of NVM content into the CFP shadow register during module initialization. Data saving from CFP shadow register to NVM is supported.
- It supports the DDM data update periodically during the whole operation of the module. The maximum data refresh period is 1 ms (real time temperature monitoring).
- It supports the whole CFP register set including all NVRs and VRs.
- Incomplete or otherwise corrupted MDIO bus transactions are purged from memory and disregarded.
- The port address is allowed to change on the fly without a module reset.

2.2 Initialization Sequence

2.2.1 I2C Frame

The Startup sequence for the **ML4030-DCO** is defined below:



Figure

MOD_RSTs assertion drives the CFP2 module to a reset state, at this stage the MDIO interface will be held in a high impedance state, the Host will read 'FFFF'h from any address, while host write operations will have no effect.
Upon the de-assertion of MOD_RSTs, the CFP2 module exists to an initialize state which is a transient state.
The Initialization time required is less than one second. When Initialization state is completed, the CFP2 module will enter a Low-Power state; at this point MDIO becomes available for R/W operations.

2.3 GLB_ALRM

Below is the flowchart for GLB_ALRM signal during CFP states transitions:

Figure

GLB _ALRM is de-asserted during Reset and Initialize state, it is asserted in Low-Power, High-Power-up, TX-Off and TX-Turn-on states, then de-asserted again when Ready state is reached. GLB_ALRMn is the hardware pin, and is the inverse of GLB_ALRM.
The below example can be run in order to check for correct module initialization and GLB_ALRM signal:

- Assert MOD_LOPWR and TX_DIS, DeassertMOD_RSTn : GLB_ALRMn should be HIGH (module in Reset state)
- Assert MOD_RSTn (module exits Reset state into Low Power state): GLB_ALRMn should be LOW
- Deassert MOD_LOPWR (module exits Low Power into TX-Off state): GLB_ALRMn should stay LOW
- Deassert TX_DIS (module enters Ready state): GLB_ALRMn should go HIGH MDIO Signals, Addressing and Frame Structure.

2.3.1 Port Address (PRTADR)

As per the port address used, the module will work on any MDIO Physical port address which can be set by the HW input signals PRTADR [2:0]. So, when using 2 or more CFP2 slots, each of them can be configured to a different Port Address.

PRTADR0	MDIO Physical Port address bit 0	I	1.2V LVCMOS
PRTADR1	MDIO Physical Port address bit 1	I	1.2V LVCMOS
PRTADR2	MDIO Physical Port address bit 2	I	1.2V LVCMOS

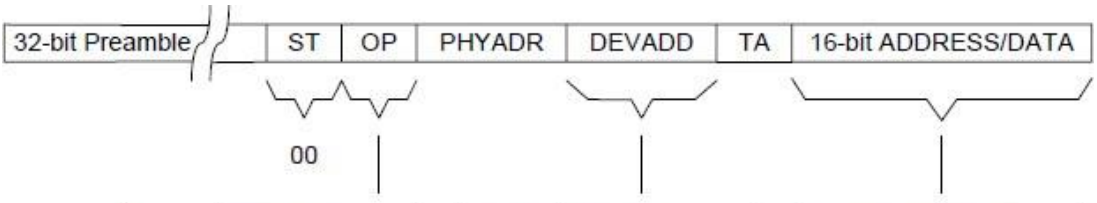
Figure

2.3.2 Device Address (DEVADD)

MDIO Device Address consists of 5 bits that are sent in MDIO frames, CFP MSA specifies that CFP register Set should be addressed using Device Address = 1, Thus CFP register space is available in the **ML4030-DCO** on D.A=1.

2.3.3 MDIO Frame

The Below Frame shows all segments of an MDIO Packet, PHYADR are the 5 bits Physical Address and DEVADD are the 5 bits Device Address.



OP	ACCESS TYPE
00	Address
01	Write
11	Read
10	Post Read Inc Add

DEVADD	DEVICE TYPE
00000	Reserved
00001	PMA/PMD
00010	WIS
00011	PCS
00100	PHY XS
00101	DTE XS

Access Type	Content
Address	Reg Address
Write	Write Data
Read	Read Data
Read Inc	Read Data

ST = start bits (2 bits),
OP = operation code (2 bits),
PHYADR = physical port address (5 bits),
DEVADD = MDIO device address (or called device type, 5 bits),
TA = turn around bits (2 bits),
16-bit ADDRESS/DATA is the payload.

Figure

2.4 CFP Register Set

All registers are supported in memory map (Refer to table below), the set of registers starting from 0x8000 to 0x9F00 are implemented as NVR registers and all these registers are always read from NVM during initialization and mapped to corresponding addresses.

All VR (Volatile Registers) are set to zero or to MSA defaults value upon module initialization.

The NVR values are saved to NVM by calling the SAVE NVR function. The base ID registers are initially set, but the user can change them if required.

Hex Addr Start	Hex Addr End	Access Type	Allocated Size	Data Bit Width	Description
0000	7FFF	N/A	32768	N/A	Reserved for IEEE 802.3 use.
8000	807F	RO	128	8	CFP NVR 1. Basic ID Registers
8080	80C6	RO	128	8	CFP NVR 2. Extended ID Registers
80C8	80FF				CFP NVR 2. MSA-100GLH Module Alarm/Warning Threshold Registers
8100	817F	RO	128	8	CFP NVR 3. Network Lane BOL Measurement Registers
8180	81FF	RO	128	8	CFP NVR 4. MSA-100GLH Extended ID Registers
8200	83FF	RO	4x128	N/A	MSA Reserved
8400	847F	RO	128	8	Vendor NVR 1. Vendor Data Registers
8480	84FF	RO	128	8	Vendor NVR 2. Vendor Data Registers
8500	87FF	RO	6x128	N/A	MSA Reserved
8800	887F	RW	128	8	User NVR 1. User Data Registers
8880	88FF	RW	128	8	User NVR 2. User Data Registers
8900	8EFF	RO	12x128	N/A	MSA Reserved
8F00	8FFF	N/A	2x128	N/A	Reserved for User private use
9000	9FFF	N/A	4096	N/A	Reserved for Vendor private use
B000	B07F	RW	128	16	MSA-100GLH Module VR1: Command/Setup/Control/FAWS Registers
B080	B17F	RO	2x128	N/A	MSA Reserved
B180	B2FF	RW	3x128	16	MSA-100GLH Module VR1: Network Lane FAWS/Status Registers
B300	B57F	RW	5x128	16	MSA-100GLH Module VR2: Network Lane Control/Data Registers
B580	B5FF	RW	128	16	MSA-100GLH Module VR2: Network Lane OTN/FEC-related Registers (Optional)
B600	B6FF	RW	2x128	16	MSA-100GLH Module VR1: Host Lane FAWS/Control/Status Registers
B700	B77F	RW	2x128	16	MSA-100GLH Module VR1: Host Lane OTN/FEC-related Registers (Optional)
B780	B7FF	RO	128	N/A	MSA Reserved
B800	BAFF	RW	6x128	16	MSA-100GLH Module VR2: Network Lane Modulation Format Dependent Registers (Optional-informative)
BB00	BBFF	RO	2x128	N/A	MSA Reserved
BC00	BFFF	RW	1024	16	MSA-100GLH Module VR2: Bulk Data Transfer Registers

Figure

2.5 User NVR Restore and Save Function (0xB004)

In order to permanently write to User NVR registers (0x8000→ 0x9F00), the host shall use the "Save" function to store the shadowed NVR data into underlying NVM. The host only needs to perform a single save operation to copy the entire User NVR shadow registers to the underlying NVM after finishing editing the data.
Upon power-up or reset the User NVR shadow registers are "Restored" with NVM values. Note that the Restore function will overwrite the NVR shadow registers, losing any host-written values in them that have occurred since the last Save to the underlying NVM.
The NVR Access Control Register (**B004h**) provides the Save function for Host to save the User NVRs content.
Bit 5 in NVR Access Control Register is designated for User NVR save command.

2.5.1 A "1" written to bit 5 in register B004h initiates a User NVR Save

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
B004	1			**NVR Access Control**		0000h
		WO	5	User Restore and Save command	1: Save the user NVR section	0

So, to call the user, NVR save command user can write 0x0020 into register 0xB004.
The Save NVR duration is around 0.5 seconds. When this function is called it should be followed by a 0.5-second time wait.
During this process the user can't write or read CFP registers.

2.6 PRG_ALRMs

The signals HIPWR_ON, MOD_READY, and MOD_FAULT are CFP internally generated signals and are defaults of the programmable alarm pins PRG_ALRMx.
The Following Table lists the corresponding functions for each of the PRG_ALRMs.

NAME	ALARM SOURCE	VALUE
HIPWR_ON	Module high-power-on indicator. PRG_ALRM1 MSA default.	0: Module not high powered up 1: Module high power up completed
MOD_READY	MOD_READY, module startup sequence done, PRG_ALRM2 MSA default.	0: Not done 1: Done
MOD_FAULT	Fault detected. PRG_ALRM3 MSA default.	0: No Fault 1: Fault

For testing purposes, PRG_ALRM3 can be manually controlled via bit 0 of register 0x9405.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9405	1			**PRG_ALRM control register**		0000h
		RW	0	PRG_ALRM3	0: De-assert PRG_ALRM3 pin 1: Assert PRG_ALRM3 pin	0

2.7 RX_LOS

The **ML4030-DCO** initially implements RX_LOS to follow TX_DIS input, assuming that in a loopback module, when the host transmitters are disabled, no data should be received thus leading to RX_LOS condition.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9404	1			**Custom Alarms**		0000h
		RW	0	Prog RX_LOS	0: RX_LOS default operation (RX_LOS= TX_DIS) 1: Programmable RX_LOS (driven as per Soft RX_LOS bit)	0
		RW	1	Soft RX_LOS	0: RX_LOS HW signal set to LOW 1: RX_LOS HW signal set to High	0

2.8 Temperature Monitor

The alarms and warnings of the CFP2 Loopback are listed in the tables below. Alarms and Warnings are set in register 0xB01F in bits 8, 9, 10 and 11, and are continuously asserted and de-asserted when the corresponding alarms/warnings occur. Addresses 0x8080, 0x8082, 0x8084, and 0x8086 are reference registers for temperature alarms and warnings, they contain the default values (HA:75, HW:65, LW:2 and LA:0) and can be changed when desired. The module is continuously reading the temperature and storing its value in Register 0xB02F.
When the temperature reaches the High Alarm values, the module front LED indicator will start blinking.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	LSB Unit
8080	2	RW	7~0	**Temp High Alarm Threshold**	These thresholds are a signed 16-bit integer with LSB = 1/256 of a degree Celsius representing a range from -128 to + 127 255/256 degree C. MSA valid range is between –40 and +125 °C. MSB stored at low address, LSB stored at high address.	1/256 degC
8082	2	RW	7~0	**Temp High Warning Threshold**		
8084	2	RO	7~0	**Temp Low Warning Threshold**		
8086	2	RO	7~0	**Temp Low Alarm Threshold**		

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
B01F	1	RO		**Module Alarms and Warnings 1**		0000h
			11	Mod Temp High Alarm	Mod temp high Alarm 0: Normal, 1: Asserted	0
			10	Mod Temp High Warning	Mod temp high Warning 0: Normal, 1: Asserted	0
			9	Mod Temp Low Warning	Mod temp high Warning 0: Normal, 1: Asserted	0
			8	Mod Temp Low Alarm	Mod temp Low Alarm 0: Normal, 1: Asserted	0

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
B02F	1	RO		**Module Temp Monitor A/D Value**	Internally measured temperature in degrees Celsius, a 16-bit signed integer with LSB = 1/256 of a degree Celsius, representing a total range from -128 to + 127 255/256 °C. MSA valid range is between –40 and +125 °C. Accuracy shall be better than +/- 3 °C over the whole temperature range.	0000h

2.9 Insertion Counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module enters an initializing sequence, as it is nonvolatile it is always saved, and can be read anytime from register 0x9400.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	LSB Unit
9400	1			**Insertion Counter**		
		RO	0~7	Insertion Count	Number of times the modules was plugged in a host	1 insertion

2.10 Programmable Power Dissipation & Thermal Emulation

Registers 0x9401, 0x9402 and 0x9403 are used for PWM control over MDIO. Those are 8-bit data registers.

The consumed power changes accordingly when the value in those registers is changed (only when in high power mode). In Low power mode the module automatically turns off PWM.

The values written in those registers can be stored by calling the Save NVR function, thus the user can permanently change the initial power consumed in high power mode when the module is powered up by setting the register value and calling the Save NVR function.

The PWM can also be used for module thermal emulation. The module contains 3 thermal spots positioned where the optical transceivers and the DSP chips usually are in an optical module that is heated relative to the related PWM register.

Note that the LED starts blinking when the temperature high alarm is reached.

2.10.1 ML4030-DCO-24W

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9401	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 8.7 W power cons	0
9402	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 7.6 W power cons	0
9403	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 7.6 W	0

					power cons	

2.10.2 ML4030-DCO-32W

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9401	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 11.35 W power cons	0
9402	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 10.37 W power cons	0
9403	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 10.37 W power cons	0

2.10.3 ML4030-DCO-36W

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
9401	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 12 W power cons	0
9402	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 12 W power cons	0
9403	1			**PWM**		
		RW	0~7	PWM	0x00 to 0xFF corresponding to 12 W power cons	0

2.11 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is defined in Register 0x9406.

The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. A Temperature Cut-Off register is defined at address 0x9406, once the module temperature reaches the cut-off temperature, the PWM will automatically turn off in order to prevent overheating. Once the module gets below cut-off value of the temperature, the PWM goes back to its previous value.

The Maximum allowed Cut-Off temperature for the **ML4030-DCO** is 90 °C, so even if the value stored in register 0x9402 is higher than 90, the module will still Cut-Off power at 90 °C. In case the value stored in 0x9402 is lower than 90, it will be adopted instead of the default value.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Default Value
9406	1			**Temp Cut-Off**		
		RW	0~7	Cut-Off Value	0x00 to 0x60 (0 to 90 °C)	0x55

2.12 Module Control and Status Registers

The below registers are implemented, and can be checked for module State and Control.

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
B010	1			**Module General Control**		0000h
		RO	15	Soft Module Reset	Register bit for module reset function. Writing a 0 to this bit has no effect regardless it was 0 or 1 previously. 1: Module reset assert	0
		RW	14	Soft Module Low Power	Register bit for module low power function. 1: Assert	0
		RW	13	Soft TX_Disable	Register bit for TX Disable function. 1: Assert	0
		RO	12-10	Reserved		0
		RW	9	Soft GLB_ALRM Test	Command bit for software forced test signal. When this bit is asserted it generates GLB_ALRM signal. 1: Assert	0
		RO	8-6	Reserved		0
		RO	5	TX_DIS Pin State	Logical state of the TX_DIS pin. 1: Assert.	0
		RO	4	MOD_LOPWR Pin State	Logical state of the MOD_LOPWR pin. 1: Assert.	0
		RO	3	PRG_CNTL3 Pin State	Logical state of the PRG_CNTL3 pin	0
		RO	2	PRG_CNTL2 Pin State	Logical state of the PRG_CNTL2 pin	0
		RO	1	PRG_CNTL1 Pin State	Logical state of the PRG_CNTL1 pin	0

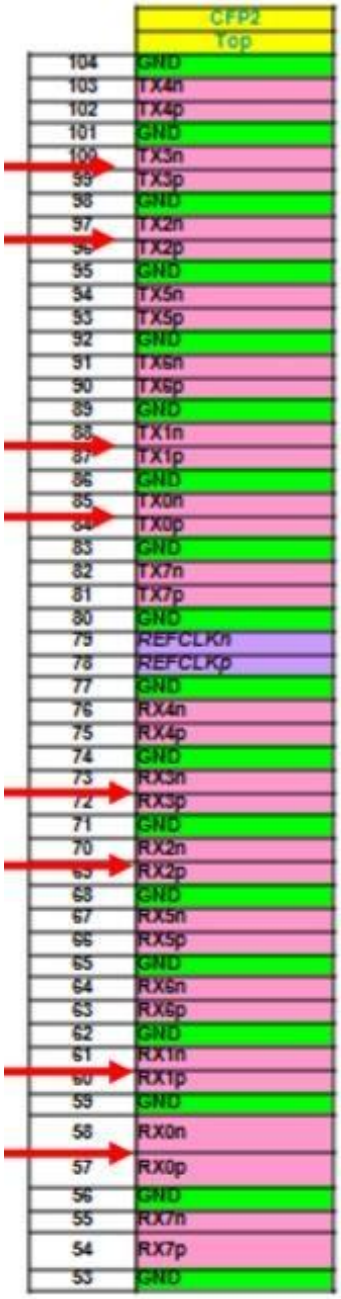
		RO	0	Reserved		0

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
B016	1			**Module State**		0000h
		RO	15~9	Reserved		0
			8	High-Power-down State	1: Corresponding state is active. Word value = 0100h.	0
			7	TX-Turn-off State	1: Corresponding state is active. Word value = 0080h.	0
			6	Fault State	1: Corresponding state is active. Word value = 0040h.	0
			5	Ready State	1: Corresponding state is active. Word value = 0020h.	0
			4	TX-Turn-on State	1: Corresponding state is active. Word value = 0010h.	0
			3	TX-Off State	1: Corresponding state is active. Word value = 0008h.	0
			2	High-Power-up State	1: Corresponding state is active. Word value = 0004h.	0
			1	Low-Power State	1: Corresponding state is active. Word value = 0002h.	0
			0	Initialize State	1: Corresponding state is active. Word value = 0001h.	0

Hex Adr	Size	Access Type	Bit	Register Name Bit Field Name	Description	Init Value
B01D	1			**Module General Status**		
		RO	1	HIPWR_ON	Status bit representing the condition of module in high power status. FAWS Type is not applicable. 0: Module is not in high power on status, 1: Module is in high powered on status.	0

3 CFP2-DCO Pin Allocation

CFP2-DCO **8x CEI 56G** pin mapping is adopted for the ML4030-DCO; the same pin mapping is compatible for using it as an Electrical loopback module for **6x CEI 56G and 4x CEI 56G**.



3.1 High Speed Signals

High speed signals are electrically looped back from the TX side to the RX side of the module, all differential TX pairs are connected to the corresponding RX pairs, and the signals are AC coupled as specified by CFP MSA HW specs.

The Passive traces connecting TX to RX pairs are designed to support a data rate up to 56 Gbps.

Revision History

Revision number	Date	Description
0.1	25/11/2016	▪ Preliminary
0.2	9/2/2021	▪ Format adjustments