USER GUIDE



Common Management Interface Kit

CMIS GUI User Guide – CMIS Rev3.0/4.0 Compliant Revision 0.2 October 2021

QSFP-DD Host – QSFP Host – DSFP Host – SFP-DD Host – OSFP Host

Innovation for the next generation



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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the General Safety Summary in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Only use the power cord specified for this product and certified for the country of use.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers.

Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate with Suspected Failures.

If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions. Do Not Operate in an Explosive Atmosphere. Keep Product Surfaces Clean and Dry

Caution statements identify conditions or practices that could result in damage to this product or other property.



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Revision Control

Revision number	Description	Release Date
0.1	 Initial version 	4/20/2020
0.22	Added CDB FeatureFormat updates	10/12/2021

List of Acronyms

Acronym	Definition
CMIS	Common Management Interface Kit
CDB	Command Data Block
BW	Bandwidth
BERT	Bit Error Rate Tester
Conf	Configuration
DUT	Device Under Test
FEC	Forward Error Correction
FW	Firmware
GBd	Gigabaud
Gbps	Gigabits per Second
GUI	Graphical User Interface
HW	Hardware
SI	Signal Integrity
Sim	Simulation
SW	Software



Introduction

The ML-CMIS GUI is a common software interface that allows to communicate with, operate and control various MCBs boards. It allows to utilize a common software across a variety of form factors. The ML-CMIS GUI communicate with the host board through USB connection. The communication is established after installing the proper driver of the target host.

The ML-CMIS GUI allows to communicate on multiple hosts simultaneously, by assigning different USB instance to each host.

The various hosts operating with the ML-CMIS GUI are listed below:

- QDD Host
- QDD host
- OSFP host
- QSFP host
- SFP-DD host
- DSFP host



GUI Introduction

1. Installation & Running

The GUI installation file is available on the website. User could download it under the target product page.

To install the GUI, simply double-click on the installer file, and follow the instructions. For Windows version newer than Windows 7 the GUI must be run as administrator. A message box will pop-up for confirmation.



Figure 1: Pop-up message

After the GUI runs properly, a window will open as shown below.

	_									Com	munication						
ulti	Lar				~~~	$\bigwedge \sim$	<u> </u>			Sele	ect Device Type:	QDD Hos	t 👻 US	B instance:		•	Module Found
~			N 4 -		~	V	1	c	12.54		Initialize	Refr	esh	Pause Mo	onitor	About Us	Module Not Four
Lon	nm	on						erface	e Kit								USB Error
			C	IMIS	Versi	on: 3.	0										
				Swite	h to C	MIS 4.0											
nitor																	
	Modu	ıle Monit	or					Interrup	t Flags								
	Ch	RX LOS	TX LOS	RX LOL	TX LOL	TX Fault	State Cng	Alarms				Warnin	gs				
	1								RX Power		TX Power		RX Power		TX Power	C	State Changed
	2							Ch 1	High Low	High Low	High Low	Ch 1	High Low	High Low	High Low		
	3							2				2					
	4							3				3					
	6							4				4					
	7							5				5					
	8							6				6					
								8				8					
	Chan	inels Mor	itor Od	Rm	() r	nW	_		High Lov	N	High Low		High Lo	w	High Low		
	Ch	RX I	Power	тх в	-	TX Pow	er	Temp		AUX 1		Temp		AUX 1			
	1							VCC 3	.3 () ()	AUX 2		VCC 3	.3 () (AUX 2			
	2							Vendor	Def 🔿 🔿	AUX 3		Vendor	Def	AUX 3			
	3							Module /	Nonitor					MCB VCC N	Nonitor	MCB C	urrent Monitor
	4							Temp		A	UX1(TEC currer	nt)		VCC:		Curren	nt VCC:
	5							Supply	3.3V	A	UX2(TEC currer	nt)		VCC1:		Curren	t VCCTX:
	6									A	UX3(Laser Temp) ((Only for	QDD-MXP)	Curren	nt VCCRX:
	7													VCCTX:			

Figure 2: GUI Window

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2. CMIS Version

The GUI covers the CMIS 3.0 and CMIS 4.0. The user must choose the CMIS version first.



Figure 3: CMIS Version Selection

By clicking on the button shown above, the user can switch between CMIS 3.0 and CMIS 4.0. Depending on the CMIS Version chosen by the user, the list of devices will change. Below is a summary of supported hosts based on CMIS version.

- CMIS Version 3.0
 - o QDD Host
 - o OSFP Hosts (ML4064-TR is under the OSFP family)
- CMIS Version 4.0
 - QDD Hosts (ML4062-TR is under the QDD family)
 - OSFP Hosts (ML4064-TR is under the OSFP family)
 - o QSFP Host
 - o SFP-DD Host
 - o DSFP Host

3. Communication

The communication between the GUI and the host is established from the Communication window. Under this window, the user can select the Device Type and the USB instance.

The connection is established by clicking the Initialize button. This button is the application main entry point. Once a USB connection is established, the Host checks if a Module is inserted, and accordingly illuminates the corresponding (Module Found or Module Not Found) LED. If a Module is inserted, the initialization process proceeds with checking the related Hardware pins to ensure that the module is selected and ready to communicate with host.

Also, the following buttons are available in the Communication window.

Refresh button: Checks for connection status, refresh Hardware Readings and updates GUI. Pause Monitor button: Pause/Resume monitoring.

About Us button: Shows software information (name, version) and company information.

Select Device Type	QDD Host -	USB instance:		Module Found
Initialize	Refresh	Pause Monitor	About Us	USB Connected
				USB Error

Figure 2: Communication Tab



4. GUI Sections

The ML-CMIS GUI contains the following tabs:

- Monitor
- Interrupt Masks
- Controls
- Low Speed Signals
- Identification
- Options Available
- Load/Save MSA
- Load/Save Page 10/11h
- I2C R/W
- I2C R/W Advanced
- DVT
- QDD-MXP (only for QSFP-DD Host)

All these tabs are common for all hosts. The subsequent sections will cover each tab separately. Any difference between various hosts in a specific tab will be mentioned explicitly.

4.1 Monitor

The Monitor tab shows the digital diagnostic monitoring flags status.

All alarms and warnings are expressed with LEDs as shown in Figure 5, when a flag is asserted, the corresponding LED turns ON (becomes red), when not asserted the LED remains transparent.

Also, the Monitor tab shows measurements of various monitoring values (voltage, current and temperature) and are displayed continuously.

Two main measurements windows are available:

- 1 Module Monitor
- 2 MCB Monitor

Note that the measured quantities differ from MCB to another depending on the implementation.

Mod	ule Monitor					Interrupt	Flags								
Ch	RX LOS TX I	OS RX LOI	TX LOL	TX Fault	State Cng	Alarms				Warnin	ps				
1							RX Power	TX Bias	TX Power		RX Power	TX Bias	TX Power	0	State Change
2						Ch	High Low	High Low	High Low	Ch	High Low	High Low	High Low		
3						1				1					
4						2				2					
1000						3				3					
5						4				4					
6						5				5					
7						6				6					
8						7				7					
						8				8					
Cha	nnels Monitor														
	C	dBm	•				High Lov		ligh Low		High Lo		High Low		
Ch	RX Pow	er TX	Bias	TX Powe	er	Temp				Temp					
1						VCC 3.	.3 O C	AUX 2		VCC 3	3 0 0	AUX 2			
2						Vendor	Def 🔿 🔿	AUX 3		Vendor	Def 🔿 🤇	AUX 3			
3						Module A	lonitor				11	MCB VCC /	Nonitor	MCB Cur	rent Monitor
4						Temp		AL	JX1(TEC curre	nt)		VCC:		Current	VCC:
5						Supply	3.3V	AU	X2(TEC curre	nt)		VCC1:		Current	VCCTX:
6									JX3(Laser Tem				QDD-MXP)		
7									marcador rom			VCCTX:		Current	Activat
												VCCIA:			Go to Set

Figure 5: Monitor Tab



The following table shows the MSA memory mapping for the monitoring tab objects.

Byte	Bit	Name	Description	Туре
14	7-	0 Module Monitor 1: Temperature MSB	Internally measured temperature: signed 2's complement in 1/256 degree Celsius increments NOTE: Temp can be below 0.	RO Opt.
15	7-	0 Module Monitor 1: Temperature1 LSB		
16	7-		Internally measured 3.3 volt input supply voltage: in 100 µV increments	RO Opt.
17	7-			
18	7-		TEC Current or Reserved monitor TEC Current: signed 2's complement in 1/32767%	RO Opt.
19	7-	0 Module Monitor 3: Aux 1 LSB	increments of maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling	
20	7-	0 Module Monitor 4: Aux 2 MSB	TEC Current or Laser Temperature monitor TEC Current: signed 2's complement in 1/32767% increments of	RO Opt.
21	7-	0 Module Monitor 4: Aux 2 LSB	maximum TEC current +32767 is max TEC current (100%) – Max Heating -32767 is min TEC current (100%) – Max Cooling Laser Temperature: signed 2's complement in 1/256 degree Celsius increments See Page 01h Byte 145 Table Table 8-30	
22	7-	MSB	Laser Temperature or additional supply voltage monitor Laser Temperature: signed 2's complement in 1/256 degree Celsius increments	RO Opt.
20		LSB	Additional supply voltage monitor: in 100 µV increments See Page 01h Byte 145 Table Table 8-30	
24	7-	MSB	Custom monitor	RO Opt.
25	7-	LSB		
8	7	L-CDB block 2 complete	Latched flag to indicate completion of the CDB command for CDB block 2. Clear on Read (See Page 01h, Byte 163 bit 7)	RO Opt.
	6	L-CDB block 1 complete	Latched flag to indicate completion of the CDB command for CDB block 1. Clear on Read (See Page 01h, Byte 163 bit 6)	RO Opt.
	5-3	Reserved		RQD
-	2	Data Path firmware fault	Some modules may contain an auxiliary device for processing the transmitted and received signals (e.g. a DSP). The Data Path Firmware Fault flag becomes set when an integrity check of the firmware for this auxiliary device finds an error.	RO Opt.
	1	Module firmware fault	The Module Firmware Fault flag becomes set when an integrity check of the module firmware finds an error. There are several possible causes of the error such as program memory becoming corrupted and incomplete firmware loading.	RO Opt.
	0	L-Module state changed flag	Latched Indication of change of Module state (see Table 8-5) Clear on Read	RO RQD
9	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag. Clear on Read	RO Opt.
	6	L-Vcc3.3v High Warning	Latched high 3.3 volts supply voltage warning flag. Clear on Read	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag. Clear on Read	
	4	L-Vcc3.3v High Alarm	Latched high 3.3 volts supply voltage alarm flag. Clear on Read	
ŀ	3	L-Temp Low Warning	Latched low temperature warning flag. Clear on Read	1
	2	L-Temp High Warning	Latched high temperature warning flag. Clear on Read	-
Γ	~			
	1	L-Temp Low Alarm	Latched low temperature alarm flag. Clear on Read	

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m	ull		ane		
г		_			
	10	7	L-Aux 2 Low Warning	Latched low warning for Aux 2 monitor. Clear on Read	RO
		6	L-Aux 2 High Warning	Latched high warning for Aux 2 monitor. Clear on Read	Opt.
		5	L-Aux 2 Low Alarm	Latched low alarm for Aux 2 monitor. Clear on Read	-
		4	L-Aux 2 High Alarm	Latched high alarm for Aux 2 monitor. Clear on Read	-
		3	L-Aux 1 Low Warning	Latched low warning for Aux 1 monitor. Clear on Read	-
		2	L-Aux 1 High Warning	Latched high warning for Aux 1 monitor. Clear on Read	-
		1	L-Aux 1 Low Alarm	Latched low alarm for Aux 1 monitor. Clear on Read	-
-		0	L-Aux 1 High Alarm	Latched high alarm for Aux 1 monitor. Clear on Read	
	11	7	L-Vendor Defined Low Warning	Latched low warning for Vendor Defined Monitor. Clear on Read	RO Opt.
		6	L-Vendor Defined High Warning	Latched high warning for Vendor Defined Monitor. Clear on Read	
		5	L-Vendor Defined Low Alarm	Latched low alarm for Vendor Defined Monitor. Clear on Read	
		4	L-Vendor Defined High Alarm	Latched high alarm for Vendor Defined Monitor. Clear on Read	
		3	L-Aux 3 Low Warning	Latched low warning for Aux 3 monitor. Clear on Read	
		2	L-Aux 3 High Warning	Latched high warning for Aux 3 monitor. Clear on Read	
		1	L-Aux 3 Low Alarm	Latched low alarm for Aux 3 monitor. Clear on Read	
		0	L-Aux 3 High Alarm	Latched high alarm for Aux 3 monitor. Clear on Read	
	12	7-0	Reserved		
	13	7-0	Custom		
	Byte	Bit	Name	Description	Туре
	134	7	L-Data Path State Changed flag, host lane 8	Latched Data Path State Changed flag for host lane 8	RO/COR RQD
		6	L-Data Path State changed flag, host lane 7	Latched Data Path State Changed flag for host lane 7	
		5	L-Data Path State Changed flag, host lane 6	Latched Data Path State Changed flag for host lane 6	
		4	L-Data Path State Changed flag, host lane 5	Latched Data Path State Changed flag for host lane 5	
		3	L-Data Path State Changed flag, host lane 4	Latched Data Path State Changed flag for host lane 4	
		2	L-Data Path State Changed flag, host lane 3	Latched Data Path State Changed flag for host lane 3	
		1	L-Data Path State Changed flag, host lane 2	Latched Data Path State Changed flag for host lane 2	
		0	L-Data Path State Changed flag, host lane 1	Latched Data Path State Changed flag for host lane 1	
Γ	135	7	L-Tx8 Fault flag	Latched Tx Fault flag, media lane 8	RO
		6	L-Tx7 Fault flag	Latched Tx Fault flag, media lane 7	Opt.
		5	L-Tx6 Fault flag	Latched Tx Fault flag, media lane 6	
		4	L-Tx5 Fault flag	Latched Tx Fault flag, media lane 5	
		3	L-Tx4 Fault flag	Latched Tx Fault flag, media lane 4	
		2	L-Tx3 Fault flag	Latched Tx Fault flag, media lane 3	
		1	L-Tx2 Fault flag	Latched Tx Fault flag, media lane 2	
		0	L-Tx1 Fault flag	Latched Tx Fault flag, media lane 1	
	136	7	L-Tx8 LOS flag	Latched Tx LOS flag, lane 8	RO
		6	L-Tx7 LOS flag	Latched Tx LOS flag, lane 7	Opt.
		5	L-Tx6 LOS flag	Latched Tx LOS flag, lane 6	
		4	L-Tx5 LOS flag	Latched Tx LOS flag, lane 5	
		3	L-Tx4 LOS flag	Latched Tx LOS flag, lane 4	
		2	L-Tx3 LOS flag	Latched Tx LOS flag, lane 3	
		1	L-Tx2 LOS flag	Latched Tx LOS flag, lane 2	
		0	L-Tx1 LOS flag	Latched Tx LOS flag, lane 1	
	137	7	L-Tx8 CDR LOL flag	Latched Tx CDR LOL flag, lane 8. Clear on Read	RO

mu	ltiL	ane		
1				
	6	L-Tx7 CDR LOL flag	Latched Tx CDR LOL flag, lane 7. Clear on Read	Opt.
	5	L-Tx6 CDR LOL flag	Latched Tx CDR LOL flag, lane 6. Clear on Read	-
	4	L-Tx5 CDR LOL flag	Latched Tx CDR LOL flag, lane 5. Clear on Read	-
	3	L-Tx4 CDR LOL flag	Latched Tx CDR LOL flag, lane 4. Clear on Read	
	2	L-Tx3 CDR LOL flag	Latched Tx CDR LOL flag, lane 3. Clear on Read	
	1	L-Tx2 CDR LOL flag	Latched Tx CDR LOL flag, lane 2. Clear on Read	
	0	L-Tx1 CDR LOL flag	Latched Tx CDR LOL flag, lane 1. Clear on Read	
13	38 7	L-Tx8 Adaptive Input Eq Fault Lane 8 flag	Latched Tx Adaptive Input Eq. Fault Lane 8. Clear on Read	RO Opt.
	6	L-Tx7 Adaptive Input Eq Fault Lane 7 flag	Latched Tx Adaptive Input Eq. Fault Lane 7. Clear on Read	
	5	L-Tx6 Adaptive Input Eq Fault Lane 6 flag	Latched Tx Adaptive Input Eq. Fault Lane 6. Clear on Read	
	4	L-Tx5 Adaptive Input Eq Fault Lane 5 flag	Latched Tx Adaptive Input Eq. Fault Lane 5. Clear on Read	
	3	L-Tx4 Adaptive Input Eq Fault Lane 4 flag	Latched Tx Adaptive Input Eq. Fault Lane 4. Clear on Read	
	2	L-Tx3 Adaptive Input Eq Fault Lane 3 flag	Latched Tx Adaptive Input Eq. Fault Lane 3. Clear on Read	
	1	L-Tx2 Adaptive Input Eq Fault Lane 2 flag	Latched Tx Adaptive Input Eq. Fault Lane 2. Clear on Read	-
	0	L-Tx1 Adaptive Input Eq Fault Lane 1 flag	Latched Tx Adaptive Input Eq. Fault Lane 1. Clear on Read	
13	39 7	L-Tx8 Power High alarm	Tx output power High Alarm, media lane 8. Clear on Read	RO
	6	L-Tx7 Power High alarm	Tx output power High Alarm, media lane 7. Clear on Read	Opt.
	5	L-Tx6 Power High alarm L-Tx5 Power High alarm	Tx output power High Alarm, media lane 6. Clear on Read Tx output power High Alarm, media lane 5. Clear on Read	-
	3	L-Tx4 Power High alarm	Tx output power High Alarm, media lane 3. Clear on Read	
	2	L-Tx3 Power High alarm	Tx output power High Alarm, media lane 3. Clear on Read	
	1	L-Tx2 Power High alarm	Tx output power High Alarm, media lane 2. Clear on Read	
	0	L-Tx1 Power High alarm	Tx output power High Alarm, media lane 1. Clear on Read	
14		L-Tx8 Power Low alarm	Tx output power Low alarm, media lane 8. Clear on Read	RO
	6	L-Tx7 Power Low alarm	Tx output power Low alarm, media lane 7. Clear on Read	Opt.
	5	L-Tx6 Power Low alarm	Tx output power Low alarm, media lane 6. Clear on Read	-
	4	L-Tx5 Power Low alarm	Tx output power Low alarm, media lane 5. Clear on Read	-
	3	L-Tx4 Power Low alarm	Tx output power Low alarm, media lane 4. Clear on Read	-
	2	L-Tx3 Power Low alarm L-Tx2 Power Low alarm	Tx output power Low alarm, media lane 3. Clear on Read Tx output power Low alarm, media lane 2. Clear on Read	-
	0	L-Tx1 Power Low alarm	Tx output power Low alarm, media lane 2. Clear on Read	-
14		L-Tx8 Power High warning	Tx output power High warning, media lane 1. Clear on Read	RO
1	6	L-Tx7 Power High warning	Tx output power High warning, media lane 0. Clear on Read	Opt.
	5	L-Tx6 Power High warning	Tx output power High warning, media lane 6. Clear on Read	opti
	4	L-Tx5 Power High warning	Tx output power High warning, media lane 5. Clear on Read	1
	3	L-Tx4 Power High warning	Tx output power High warning, media lane 4. Clear on Read	
	2	L-Tx3 Power High warning	Tx output power High warning, media lane 3. Clear on Read	te Windov
	1	L-Tx2 Power High warning	Tx output power High warning, media lane 2. Clear on Readse	ettings to activ
	0	L-Tx1 Power High warning	Tx output power High warning, media lane 1. Clear on Read	
14	12 7	L-Tx8 Power Low warning	Tx output power Low warning, media lane 8. Clear on Read	RO
	6	L-Tx7 Power Low warning	Tx output power Low warning, media lane 7. Clear on Read	Opt.
	5	L-Tx6 Power Low warning	Tx output power Low warning, media lane 6. Clear on Read	
	4	L-Tx5 Power Low warning	Tx output power Low warning, media lane 5. Clear on Read	

m	ult	iĻ	ane		
_					
		3	L-Tx4 Power Low warning	Tx output power Low warning, media lane 4. Clear on Read	
		2	L-Tx3 Power Low warning	Tx output power Low warning, media lane 3. Clear on Read	
		1	L-Tx2 Power Low warning	Tx output power Low warning, media lane 2. Clear on Read	
		0	L-Tx1 Power Low warning	Tx output power Low warning, media lane 1. Clear on Read	
	143	7	L-Tx8 Bias High Alarm	Tx Bias High Alarm, media lane 8. Clear on Read	RO
		6	L-Tx7 Bias High Alarm	Tx Bias High Alarm, media lane 7. Clear on Read	Opt.
		5	L-Tx6 Bias High Alarm	Tx Bias High Alarm, media lane 6. Clear on Read	
		4	L-Tx5 Bias High Alarm	Tx Bias High Alarm, media lane 5. Clear on Read	
		3	L-Tx4 Bias High Alarm	Tx Bias High Alarm, media lane 4. Clear on Read	
		2	L-Tx3 Bias High Alarm	Tx Bias High Alarm, media lane 3. Clear on Read	
		1	L-Tx2 Bias High Alarm	Tx Bias High Alarm, media lane 2. Clear on Read	
		0	L-Tx1 Bias High Alarm	Tx Bias High Alarm, media lane 1. Clear on Read	
	144	7	L-Tx8 Bias Low alarm	Tx Bias Low alarm, media lane 8. Clear on Read	RO
		6	L-Tx7 Bias Low alarm	Tx Bias Low alarm, media lane 7. Clear on Read	Opt.
		5	L-Tx6 Bias Low alarm	Tx Bias Low alarm, media lane 6. Clear on Read	
		4	L-Tx5 Bias Low alarm	Tx Bias Low alarm, media lane 5. Clear on Read	
		3	L-Tx4 Bias Low alarm	Tx Bias Low alarm, media lane 4. Clear on Read	
		2	L-Tx3 Bias Low alarm	Tx Bias Low alarm, media lane 3. Clear on Read	
		1	L-Tx2 Bias Low alarm	Tx Bias Low alarm, media lane 2. Clear on Read	
		0	L-Tx1 Bias Low alarm	Tx Bias Low alarm, media lane 1. Clear on Read	
	145	7	L-Tx8 Bias High warning	Tx Bias High warning, media lane 8. Clear on Read	RO
		6	L-Tx7 Bias High warning	Tx Bias High warning, media lane 7. Clear on Read	Opt.
		5	L-Tx6 Bias High warning	Tx Bias High warning, media lane 6. Clear on Read	
		4	L-Tx5 Bias High warning	Tx Bias High warning, media lane 5. Clear on Read	
		3	L-Tx4 Bias High warning	Tx Bias High warning, media lane 4. Clear on Read	
		2	L-Tx3 Bias High warning	Tx Bias High warning, media lane 3. Clear on Read	
		1	L-Tx2 Bias High warning	Tx Bias High warning, media lane 2. Clear on Read	
		0	L-Tx1 Bias High warning	Tx Bias High warning, media lane 1. Clear on Read	
	146	7	L-Tx8 Bias Low warning	Tx Bias Low warning, media lane 8. Clear on Read	RO
		6	L-Tx7 Bias Low warning	Tx Bias Low warning, media lane 7. Clear on Read	Opt.
		5	L-Tx6 Bias Low warning	Tx Bias Low warning, media lane 6. Clear on Read	
		4	L-Tx5 Bias Low warning	Tx Bias Low warning, media lane 5. Clear on Read	
		3	L-Tx4 Bias Low warning	Tx Bias Low warning, media lane 4. Clear on Read	
		2	L-Tx3 Bias Low warning	Tx Bias Low warning, media lane 3. Clear on Read	
		1	L-Tx2 Bias Low warning	Tx Bias Low warning, media lane 2. Clear on Read	
		0	L-Tx1 Bias Low warning	Tx Bias Low warning, media lane 1. Clear on Read	
	147	7	L-Rx8 LOS	Latched Rx LOS flag, media lane 8. Clear on Read	RO
		6	L-Rx7 LOS	Latched Rx LOS flag, media lane 7. Clear on Read	Opt.
		5	L-Rx6 LOS	Latched Rx LOS flag, media lane 6. Clear on Read	7
		4	L-Rx5 LOS	Latched Rx LOS flag, media lane 5. Clear on Read	1
		3	L-Rx4 LOS	Latched Rx LOS flag, media lane 4. Clear on Read	7
		2	L-Rx3 LOS	Latched Rx LOS flag, media lane 3. Clear on Read	7
		1	L-Rx2 LOS	Latched Rx LOS flag, media lane 2. Clear on Read	1
		0	L-Rx1 LOS	Latched Rx LOS flag, media lane 1. Clear on Read	1
ŀ	148	7	L-Rx8 CDR LOL	Latched Rx CDR LOL flag, media lane 8. Clear on Read	RO
		6	L-Rx7 CDR LOL	Latched Rx CDR LOL flag, media lane 7. Clear on Read	Opt.
		5	L-Rx6 CDR LOL	Latched Rx CDR LOL flag, media lane 6. Clear on Read	
		4	L-Rx5 CDR LOL	Latched Rx CDR LOL flag, media lane 5. Clear on Read	1
		3	L-Rx4 CDR LOL	Latched Rx CDR LOL flag, media lane 4. Clear on Read	1
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1 1	2	L-Rx3 CDR LOL		Latched Rx CDR LOL flag, media lane 3. Clear on Read	
	1	L-Rx2 CDR LOL		Latched Rx CDR LOL flag, media lane 2. Clear on Read	
	0	L-Rx1 CDR LOL		Latched Rx CDR LOL flag, media lane 1. Clear on Read	
149	7	L-Rx8 Power High alar	m	Rx input power High alarm, media lane 8. Clear on Read	RO
	6	L-Rx7 Power High alar		Rx input power High alarm, media lane 7. Clear on Read	Opt.
	5	L-Rx6 Power High alar		Rx input power High alarm, media lane 6. Clear on Read	opt.
	4	L-Rx5 Power High alar		Rx input power High alarm, media lane 5. Clear on Read	
	3	L-Rx4 Power High alar		Rx input power High alarm, media lane 4. Clear on Read	
	2	L-Rx3 Power High alar		Rx input power High alarm, media lane 3. Clear on Read	
	1	L-Rx2 Power High alar		Rx input power High alarm, media lane 3. Clear on Read	
	0	L-Rx1 Power High alar		Rx input power High alarm, media lane 1. Clear on Read	
150	7	L-Rx8 Power Low alarn		Rx input power Low alarm, media lane 8. Clear on Read	RO
150	6	L-Rx7 Power Low alarr		Rx input power Low alarm, media lane 7. Clear on Read	Opt.
	5	L-Rx6 Power Low alarn		Rx input power Low alarm, media lane 6. Clear on Read	opt.
	4	L-Rx5 Power Low alarr		Rx input power Low alarm, media lane 5. Clear on Read	
	3	L-Rx4 Power Low alarr		Rx input power Low alarm, media lane 4. Clear on Read	
	2	L-Rx3 Power Low alarr		Rx input power Low alarm, media lane 4. Clear on Read	
	1	L-Rx2 Power Low alarr		Rx input power Low alarm, media lane 5. Clear on Read	
	0	L-Rx1 Power Low alarr		Rx input power Low alarm, media lane 2. Clear on Read	
151	7	L-Rx8 Power High war			RO
151	6	L-Rx7 Power High war		Rx input power High warning, media lane 8. Clear on Read	Opt.
	5	L-Rx6 Power High war		Rx input power High warning, media lane 7. Clear on Read Rx input power High warning, media lane 6. Clear on Read	Opt.
	5 4	L-Rx5 Power High war		Rx input power High warning, media lane 5. Clear on Read	
	3	L-Rx4 Power High war		Rx input power High warning, media lane 4. Clear on Read	
	2	L-Rx3 Power High war		Rx input power High warning, media lane 3. Clear on Read	
-	0	L-Rx2 Power High war		Rx input power High warning, media lane 2. Clear on Read	
150	7	L-Rx1 Power High war		Rx input power High warning, media lane 1. Clear on Read	DO
152		L-Rx8 Power Low warr		Rx input power Low warning, media lane 8. Clear on Read	RO
	6	L-Rx7 Power Low warr		Rx input power Low warning, media lane 7. Clear on Read	Opt.
	5	L-Rx6 Power Low warr		Rx input power Low warning, media lane 6. Clear on Read	
	4	L-Rx5 Power Low warr		Rx input power Low warning, media lane 5. Clear on Read	
	3	L-Rx4 Power Low warr		Rx input power Low warning, media lane 4. Clear on Read	
	2	L-Rx3 Power Low warr		Rx input power Low warning, media lane 3. Clear on Read	
-	1	L-Rx2 Power Low warr		Rx input power Low warning, media lane 2. Clear on Read	
	0	L-Rx1 Power Low warr		Rx input power Low warning, media lane 1. Clear on Read	
Byte	Bit	Name	Descripti	on	Туре
153	7-0	Reserved			RO
154	7-0	Tx1 Power MSB		measured Tx output optical power: unsigned integer in 0.1	RO
155	7-0	Tx1 Power LSB		nents, yielding a total measurement range of 0 to 6.5535	Opt.
156	7-0	Tx2 Power MSB	mw (~-40) to +8.2 dBm)	
157	7-0	Tx2 Power LSB			
158	7-0	Tx3 Power MSB			
159	7-0	Tx3 Power LSB			
160	7-0	Tx4 Power MSB			
161	7-0	Tx4 Power LSB			
162	7-0	Tx5 Power MSB			
163	7-0	Tx5 Power LSB			
164	7-0	Tx6 Power MSB			
165	7-0	Tx6 Power LSB			
166	7-0	Tx7 Power MSB			
167	7-0	Tx7 Power LSB			
168	7-0	Tx8 Power MSB			
169	7-0	Tx8 Power LSB			

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170	7-0	Tx1 Bias MSB	Internally measured Tx bias current monitor: unsigned integer in 2 uA	RO
171	7-0	Tx1 Bias LSB	increments, times the multiplier from Table 8-33.	Opt.
172	7-0	Tx2 Bias MSB		
173	7-0	Tx2 Bias LSB		
174	7-0	Tx3 Bias MSB		
175	7-0	Tx3 Bias LSB		
176	7-0	Tx4 Bias MSB		
177	7-0	Tx4 Bias LSB		
178	7-0	Tx5 Bias MSB		
179	7-0	Tx5 Bias LSB		
180	7-0	Tx6 Bias MSB		
181	7-0	Tx6 Bias LSB		
182	7-0	Tx7 Bias MSB		
183	7-0	Tx7 Bias LSB		
184	7-0	Tx8 Bias MSB		
185	7-0	Tx8 Bias LSB		
186	7-0	Rx1 Power MSB	Internally measured Rx input optical power:	RO
187	7-0	Rx1 Power LSB	unsigned integer in 0.1 uW increments, yielding a total measurement	Opt.
188	7-0	Rx2 Power MSB	range of 0 to 6.5535 mW (~-40 to +8.2 dBm)	
189	7-0	Rx2 Power LSB		
190	7-0	Rx3 Power MSB		
191	7-0	Rx3 Power LSB		
192	7-0	Rx4 Power MSB		
193	7-0	Rx4 Power LSB		
194	7-0	Rx5 Power MSB		
195	7-0	Rx5 Power LSB		
196	7-0	Rx6 Power MSB		
197	7-0	Rx6 Power LSB		
198	7-0	Rx7 Power MSB		
199	7-0	Rx7 Power LSB		
200	7-0	Rx8 Power MSB		
201	7-0	Rx8 Power LSB		

4.2 Interrupt Masks

Masks shown in this tab are used to prevent a specified flag of generating an interrupt (IntL) when asserted and prevent continued interruption from on-going conditions.

When a mask is set, an interrupt will not be asserted by the corresponding (Alarm/Warning) latched flag bit.

All Masking bits are volatile and will be reset (set to 0) on module startup.

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Lane-Spe	cific Fla	g Masks		_			High		High		High L		Ch	High			Low		Low	
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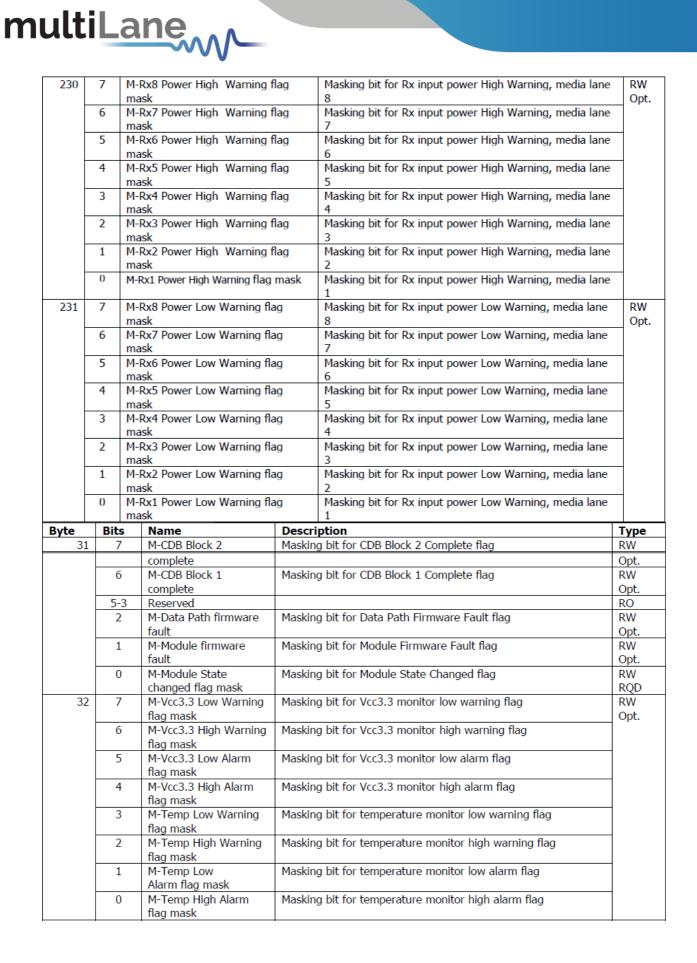
Figure 3: Interrupt Masks Tab

The table below shows the corresponding MSA mapping for the interrupt flags.

Byte	Bits	Name	Description	Тур
213	7	M- Data Path State Changed flag mask, host lane 8	Masking bit for Data Path State Changed flag, host lane 8	RW RQD
ŀ	6	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 7	
	0	mask, host lane 7	Masking bit for Data Path State Changed hag, nost lane 7	
ŀ	5	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 6	-
	5	mask, host lane 6	Hasking bit for Data Path State changed hag, host lane o	
ŀ	4	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 5	1
	т	mask, host lane 5	Hasking bit for Data Path State Changed hag, host lane 5	
ŀ	3	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 4	1
	5	mask, host lane 4	Hasking bit for Data Path State Changed hag, host lane 4	
ŀ	2	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 3	1
	2	mask, host lane 3	Plasking bit for bata r aut state changed hag, host lane s	
ŀ	1	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 2	1
	1	mask, host lane 2	Plasting bit for bata rath state changed hag, host lane z	
ŀ	0	M-Data Path State Changed flag	Masking bit for Data Path State Changed flag, host lane 1	1
	0	mask, host lane 1	Plasking bit for bata r att state changed hag, host lane 1	
214	7	M-Tx8 Fault flag mask	Masking bit for Tx Fault flag, media lane 8	RW
211	6	M-Tx7 Fault flag mask	Masking bit for Tx Fault flag, media lane 7	Opt
ŀ	5	M-Tx6 Fault flag mask	Masking bit for Tx Fault flag, media lane 6	
ŀ	4	M-Tx5 Fault flag mask	Masking bit for Tx Fault flag, media lane 5	1
ŀ	3	M-Tx4 Fault flag mask	Masking bit for Tx Fault flag, media lane 4	1
ŀ	2	M-Tx3 Fault flag mask	Masking bit for Tx Fault flag, media lane 3	1
ŀ	1	M-Tx2 Fault flag mask	Masking bit for Tx Fault flag, media lane 2	1
ŀ	0	M-Tx1 Fault flag mask	Masking bit for Tx Fault flag, media lane 1	1
215	7	M-Tx8 LOS flag mask	Masking bit for Tx LOS flag, lane 8	RW
215	6	M-Tx7 LOS flag mask	Masking bit for Tx LOS flag, lane 7	Opt
ŀ	5	M-Tx7 LOS flag mask	Masking bit for Tx LOS flag, lane 7 Masking bit for Tx LOS flag, lane 6	
ŀ	4	M-Tx5 LOS flag mask	Masking bit for Tx LOS flag, lane 5	-
ŀ				-
ŀ	3	M-Tx4 LOS flag mask M-Tx3 LOS flag mask	Masking bit for Tx LOS flag, lane 4 Masking bit for Tx LOS flag, lane 3	-
ŀ		M-Tx3 LOS flag mask		-
ŀ	1 0		Masking bit for Tx LOS flag, lane 2	-
210		M-Tx1 LOS flag mask	Masking bit for Tx LOS flag, lane 1	DW
216	7	M-Tx8 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 8	RW
ŀ	6	M-Tx7 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 7	Opt
ŀ	5	M-Tx6 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 6	-
ŀ	4	M-Tx5 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 5	-
ŀ	3	M-Tx4 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 4 Masking bit for Tx CDR LOL flag, lane 3	-
ŀ	2	M-Tx3 CDR LOL flag mask		-
ŀ	1	M-Tx2 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 2	-
047	0	M-Tx1 CDR LOL flag mask	Masking bit for Tx CDR LOL flag, lane 1	-
217		M-Tx8 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 8	RW
ŀ	6	M-Tx7 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 7	Opt
ŀ	5	M-Tx6 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 6	-
ļ	4	M-Tx5 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 5	-
ļ	3	M-Tx4 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 4	4
ļ	2	M-Tx3 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 3	-
ļ	1	M-Tx2 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 2	4
	0	M-Tx1 Adaptive Eq Fault flag mask	Masking bit for Tx Adaptive Input Eq Fail lane 1	
218	7	M-Tx8 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 8	RW
	6	M-Tx7 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 7	Opt

mult		200		
muu		ane		
I	5	M-Tx6 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 6	
	4	M-Tx5 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 5	1
	3	M-Tx4 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 4]
	2	M-Tx3 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 3	
	1	M-Tx2 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 2	
	0	M-Tx1 Power High Alarm flag mask	Masking bit for Tx output power High Alarm, media lane 1	
219	7	M-Tx8 Power Low Alarm flag mask M-Tx7 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 8	RW Opt.
	5	M-Tx6 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 7 Masking bit for Tx output power Low Alarm, media lane 6	Opt.
	4	M-Tx5 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 5	-
	3	M-Tx4 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 4	1
	2	M-Tx3 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 3	1
	1	M-Tx2 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 2]
	0	M-Tx1 Power Low Alarm flag mask	Masking bit for Tx output power Low Alarm, media lane 1	
220	7	M-Tx8 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 8	RW Opt.
	6	M-Tx7 Power High Warning flag	Masking bit for Tx output power High Warning,	
	5	mask M-Tx6 Power High Warning flag	media lane 7 Masking bit for Tx output power High Warning,	-
	5	mask	media lane 6	
	4	M-Tx5 Power High Warning flag	Masking bit for Tx output power High Warning,	1
		mask	media lane 5	
	3	M-Tx4 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 4	
	2	M-Tx3 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 3	
	1	M-Tx2 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 2	
	0	M-Tx1 Power High Warning flag mask	Masking bit for Tx output power High Warning, media lane 1	
221	7	M-Tx8 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 8	RW Opt.
	6	M-Tx7 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 7	
	5	M-Tx6 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 6	
	4	M-Tx5 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 5	
	3	M-Tx4 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 4	
	2	M-Tx3 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 3	
	1	M-Tx2 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 2	
	0	M-Tx1 Power Low Warning flag mask	Masking bit for Tx output power Low Warning, media lane 1	
222	7	M-Tx8 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 8	RW
	6	M-Tx7 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 7	Opt.
	5	M-Tx6 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 6	4
	4	M-Tx5 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 5	
	3	M-Tx4 Bias High Alarm flag mask M-Tx3 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 4 Masking bit for Tx bias High Alarm, media lane 3	
	1	M-Tx2 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 3 Masking bit for Tx bias High Alarm, media lane 2	
	0	M-Tx1 Bias High Alarm flag mask	Masking bit for Tx bias High Alarm, media lane 2	

223	7	M Tv9 Pigg Low Alarm flag mack	Masking bit for Tx bias Low Alarm, media lane 8	RW
225	7 6	M-Tx8 Bias Low Alarm flag mask M-Tx7 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 7	Opt.
F	5	M-Tx6 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 6	opt.
F	4	M-Tx5 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 5	-
F	3	M-Tx4 Bias Low Alarm flag mask	Masking bit for Tx bias Low Alarm, media lane 4	-
F	2	M-Tx4 Blas Low Alarm flag mask		-
F	1		Masking bit for Tx bias Low Alarm, media lane 3	-
F	0	M-Tx2 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 2	-
224		M-Tx1 Bias Low Alarm flag mask	Masking bit for Tx Bias Low Alarm, media lane 1	DW
224	7	M-Tx8 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 8	RW Opt.
F	6	M-Tx7 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 7	opt.
F	5 4	M-Tx6 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 6	-
F		M-Tx5 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 5	-
F	3	M-Tx4 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 4	-
F	2	M-Tx3 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 3	-
F	1	M-Tx2 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 2	-
	0	M-Tx1 Bias High Warning flag mask	Masking bit for Tx Bias High Warning, media lane 1	
225	7	M-Tx8 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 8	RW
	6	M-Tx7 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 7	Opt.
	5	M-Tx6 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 6	4
F	4	M-Tx5 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 5	4
L	3	M-Tx4 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 4	4
L	2	M-Tx3 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 3	4
L	1	M-Tx2 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 2	4
	0	M-Tx1 Bias Low Warning flag mask	Masking bit for Tx Bias Low Warning, media lane 1	
226	7	M-Rx8 LOS flag mask	Masking bit for Rx LOS flag, media lane 8	RW
	6	M-Rx7 LOS flag mask	Masking bit for Rx LOS flag, media lane 7	Opt.
	5	M-Rx6 LOS flag mask	Masking bit for Rx LOS flag, media lane 6	
	4	M-Rx5 LOS flag mask	Masking bit for Rx LOS flag, media lane 5	
	3	M-Rx4 LOS flag mask	Masking bit for Rx LOS flag, media lane 4	
	2	M-Rx3 LOS flag mask	Masking bit for Rx LOS flag, media lane 3	
	1	M-Rx2 LOS flag mask	Masking bit for Rx LOS flag, media lane 2	
	0	M-Rx1 LOS flag mask	Masking bit for Rx LOS flag, media lane 1	
227	7	M-Rx8 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 8	RW
	6	M-Rx7 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 7	Opt.
Γ	5	M-Rx6 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 6	
	4	M-Rx5 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 5	1
	3	M-Rx4 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 4	1
	2	M-Rx3 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 3	1
F	1	M-Rx2 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 2	1
F	0	M-Rx1 CDR LOL flag mask	Masking bit for Rx CDR LOL flag, media lane 1	1
228	7	M-Rx8 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 8	RW
	6	M-Rx7 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 7	Opt.
F	5	M-Rx6 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 6	1 '
F	4	M-Rx5 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 5	1
F	3	M-Rx4 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 4	1
F	2	M-Rx3 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 3	1
F	1	M-Rx2 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 2	1
F	0	M-Rx1 Power High Alarm flag mask	Masking bit for Rx input power High Alarm, media lane 1	1
229	7	M-Rx8 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 8	RW
~~ ~	6	M-Rx7 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 7	Opt.
⊢	5	M-Rx7 Power Low Alarm hag mask M-Rx6 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 6	- ^{opt.}
	4	M-Rx5 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 5	-
-	3	M-Rx4 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 4	
		M D O D D D D D D D D D D D D D D D D D	Mandata and the face Decision of the second state of the second st	
	2	M-Rx3 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 3	_
-		M-Rx3 Power Low Alarm flag mask M-Rx2 Power Low Alarm flag mask	Masking bit for Rx input power low Alarm, media lane 3 Masking bit for Rx input power low Alarm, media lane 2	



33	7	M-Aux 2 Low Warning flag mask	Masking bit for Aux 2 monitor low warning flag	RW Opt.
	6	M-Aux 2 High Warning flag mask	Masking bit for Aux 2 monitor high warning flag	
	5	M-Aux 2 Low Alarm flag mask	Masking bit for Aux 2 monitor low alarm flag	
	4	M-Aux 2 High Alarm flag mask	Masking bit for Aux 2 monitor high alarm flag	
	3	M-Aux 1 Low Warning flag mask	Masking bit for Aux 1 monitor low warning flag	
	2	M-Aux 1 High Warning flag mask	Masking bit for Aux 1 monitor high warning flag	
	1	M-Aux 1 Low Alarm flag mask	Masking bit for Aux 1 monitor low alarm flag	
	0	M-Aux 1 High Alarm flag mask	Masking bit for Aux 1 monitor high alarm flag	
34	7	M-Vendor Defined Low Warning flag mask	Masking bit for Vendor defined low warning flag	RW Opt.
	6	M-Vendor Defined High Warning flag mask	Masking bit for Vendor defined high warning flag	
	5	M-Vendor Defined Low Alarm flag mask	Masking bit for Vendor defined low alarm flag	
	4	M-Vendor Defined High Alarm flag mask	Masking bit for Vendor defined high alarm flag	
	3	M-Aux 3 Low Warning flag mask	Masking bit for Aux 3 monitor low warning flag	
	2	M-Aux 3 High Warning	Masking bit for Aux 3 monitor high warning flag	
		flag mask		
	1	M-Aux 3 Low Alarm flag mask	Masking bit for Aux 3 monitor low alarm flag	
	0	M-Aux 3 High Alarm flag mask	Masking bit for Aux 3 monitor high alarm flag	
35	7-0	Reserved flag mask		
36	7-0	Custom	Module level flag masks	

4.3 Controls

The control fields allow the host to dynamically change the behavior of the device. It allows the user to control Tx Input Equalization, Rx amplitude, Rx Pre-Cursor and Rx Post-Cursor.

The User should follow this procedure:

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- Set values to the control fields.
- Apply the configuration by selecting either ApplyDataPathInit or ApplyImmmediate.
- Press one of the 2 buttons (Apply All or Apply Lane) depending on user need.
- The module copies the data to the Active set.
- If the DataPathPwrUp is set, this applied configuration will be applied to the hardware.

Also this tab allows the user to control the module voltage, in case of the MCB is supplied by dual supply (5V and 3.3V). Three voltage levels are available: 3.15V, 3.3V and 3.45V.



Host VCC				
Set Host VCC:	🔿 3.15V	● 3.3V	3.45V	Note: This option is effective if the host is powered by 5V only.

Figure 4: MCB Voltage Control

Click to refresh	this page Refr	esh Page Host V Set Ho	cc st VCC: 0 3.15V	● 3.3V 〇	3.45V Note: Thi	is option is effective if	the host is powered by	5V only.
x Output Disable	Tx Polarity Flip	Tx Squelch Disable	Tx Force Squelch	Tx Flag Squelch	Rx Polarity Flip	Rx Output Disable	Rx Squelch Disable	Rx Flag Squelch
Tx1	Tx1	Tx1	Tx1	Tx1	Rx1	Rx1	Rx1	Rx1
Tx2	Tx2	Tx2	Tx2	Tx2	Rx2	Rx2	Rx2	Rx2
Tx3	Tx3	Tx3	Tx3	Tx3	Rx3	Rx3	Rx3	Rx3
Tx4	Tx4	Tx4	Tx4	Tx4	Rx4	Rx4	Rx4	Rx4
Tx5	Tx5	Tx5	Tx5	Tx5	Rx5	Rx5	Rx5	Rx5
Tx6	Tx6	Tx6	Tx6	Tx6	Rx6	Rx6	Rx6	Rx6
Tx7	Tx7	Tx7	Tx7	Tx7	🔲 Rx7	🔲 Rx7	Rx7	Rx7
Tx8	Tx8	Tx8	Tx8	Tx8	Rx8	Rx8	Rx8	Rx8
x Input Equalization		Rx Output Amplitude	Rx Output Pre-cu	irsor	Rx Output Post-c	ursor	Apply Data	DataPathPwrUp
x1 U	0 dB	Rx1 mV		0 dB		0 dB	 ApplyDataPathInit 	Ch1
···· • • • • • • • • • • • • • • • • •		Rx1 mV	Rx1		Rx1 🔍		ApplyImmediate	Ch2
x2 U	0 dB	Rx2 mV	Rx2	0 dB	Rx2	0 dB		Ch3
x3 U	0 dB	Rx3 mV	Rx3	0 dB	Rx3	0 dB	Apply Lane	Ch4
T			· · · · · · · · · · · · · · · · · · ·	0 dB	· · · · · ·		Apply All	Ch5
「x4 ₩	0 dB	Rx4 • mV	Rx4	0 dB	Rx4	0 dB		Ch6
rx5 U	0 dB	Rx5 🚽 mV	Rx5	0 dB	Rx5	0 dB		Ch7
x6 U	0 dB	Rx6 mV	Rx6	0 dB	Rx6	0 dB		Ch8
rx7 U	0 дв	Rx7mV	Rx7	0 dB	Rx7	о дв		
M Y	U UB		KX/	0 00	KX/	0 00		

Figure 5: Control Tab

The following table shows the corresponding registers, along with their names and description.

Byte	Bit	Name	Description	Туре
128	7	DataPathDeinit Host Lane 8	Data Path initialization control for host lane 8	RW
			0b=Initialize the data path associated with host lane 8	RQD
			1b=Deinitialize the data path associated with host lane 8	
	6	DataPathDeinit Host Lane 7	Data Path initialization control for host lane 7	
			0b=Initialize the data path associated with host lane 7	
			1b=Deinitialize the data path associated with host lane 7	
	5	DataPathDeinit Host Lane 6	Data Path initialization control for host lane 6	
			0b=Initialize the data path associated with host lane 6	
			1b=Deinitialize the data path associated with host lane 6	
	4	DataPathDeinit Host Lane 5	Data Path initialization control for host lane 5	
			0b=Initialize the data path associated with host lane 5	
			1b= Deinitialize the data path associated with host lane 5	
	3	DataPathDeinit Host Lane 4	Data Path initialization control for host lane 4	
			0b=Initialize the data path associated with host lane 4	
			1b=Deinitialize the data path associated with host lane 4	
	2	DataPathDeinit Host Lane 3	Data Path initialization control for host lane 3	
			0b=Initialize the data path associated with host lane 4	
			1b=Deinitialize the data path associated with host lane 3	
	1	DataPathDeinit Host Lane 2	Data Path initialization control for host lane 2	
			0b=Initialize the data path associated with host lane 2	
			1b=Deinitialize the data path associated with host lane 2	
	0	DataPathDeinit Host Lane 1	Data Path initialization control for host lane 1	
			0b=Initialize the data path associated with host lane 1	
			1b=Deinitialize the data path associated with host lane 1	



129	7	Tx8 Polarity Flip	0b=No polarity flip for lane 8 1b=Tx input polarity flip for lane 8	RW Opt
F	6	Tx7 Polarity Flip	0b=No polarity flip for lane 7	
			1b=Tx input polarity flip for lane 7	
	5	Tx6 Polarity Flip	0b=No polarity flip for lane 6	
			1b=Tx input polarity flip for lane 6	
Γ	4	Tx5 Polarity Flip	0b=No polarity flip for lane 5	
			1b=Tx input polarity flip for lane 5	
Γ	3	Tx4 Polarity Flip	0b=No polarity flip for lane 4	
			1b=Tx input polarity flip for lane 4	
Γ	2	Tx3 Polarity Flip	0b=No polarity flip for lane 3	
			1b=Tx input polarity flip for lane 3	
	1	Tx2 Polarity Flip	0b=No polarity flip for lane 2	
			1b=Tx input polarity flip for lane 2	
	0	Tx1 Polarity Flip	0b=No polarity flip for lane 1	
			1b=Tx input polarity flip for lane 1	
130	7	Tx8 Disable	0b=Tx output enabled for media lane 8	RW
			1b=Tx output disabled for media lane 8	Opt
Γ	6	Tx7 Disable	0b=Tx output enabled for media lane 7	
L			1b=Tx output disabled for media lane 7	
	5	Tx6 Disable	0b=Tx output enabled for media lane 6	
			1b=Tx output disabled for media lane 6	
	4	Tx5 Disable	0b=Tx output enabled for media lane 5	
			1b=Tx output disabled for media lane 5	
	3	Tx4 Disable	0b=Tx output enabled for media lane 4	
			1b=Tx output disabled for media lane 4	
	2	Tx3 Disable	0b=Tx output enabled for media lane 3	
			1b=Tx output disabled for media lane 3	
	1	Tx2 Disable	0b=Tx output enabled for media lane 2	
			1b=Tx output disabled for media lane 2	
	0	Tx1 Disable	0b=Tx output enabled for media lane 1	
			1b=Tx output disabled for media lane 1	
131	7	Tx8 Squelch Disable	0b=Tx output squelch permitted for media lane 8 when	RW
			associated host input LOS is detected	Opt
L			1b=Tx output squelch not permitted for media lane 8	
	6	Tx7 Squelch Disable	0b=Tx output squelch permitted for media lane 7 when	
			associated host input LOS is detected	
L			1b=Tx output squelch not permitted for media lane 7	
	5	Tx6 Squelch Disable	0b=Tx output squelch permitted for media lane 6 when	
			associated host input LOS is detected	
Ļ			1b=Tx output squelch not permitted for media lane 6	
	4	Tx5 Squelch Disable	0b=Tx output squelch permitted for media lane 5 when	
			associated host input LOS is detected	
Ļ			1b=Tx output squelch not permitted for media lane 5	
	3	Tx4 Squelch Disable	0b=Tx output squelch permitted for media lane 4 when	
			associated host input LOS is detected	
┝	~	Tra Crushk St. 11	1b=Tx output squelch not permitted for media lane 4	
	2	Tx3 Squelch Disable	0b=Tx output squelch permitted for media lane 3 when	
			associated host input LOS is detected	
⊢	4	Ty2 Caualab Disable	1b=Tx output squelch not permitted for media lane 3	
	1	Tx2 Squelch Disable	0b=Tx output squelch permitted for media lane 2 when	
			associated host input LOS is detected	
┝	0	Tut Caualab Dischla	1b=Tx output squelch not permitted for media lane 2	
	0	Tx1 Squelch Disable	0b=Tx output squelch permitted for media lane 1 when	
			associated host input LOS is detected	
1			1b=Tx output squelch not permitted for media lane 1	



132	7	Tx8 Force Squelch	0b=No impact on Tx behavior for media lane 8	RW
		775 0 11	1b=Tx output squelched for media lane 8	Opt.
	6	Tx7 Force Squelch	0b=No impact on Tx behavior for media lane 7 1b=Tx output squelched for media lane 7	
	5	Tx6 Force Squelch	0b=No impact on Tx behavior for media lane 6	-
	0	The Force equelen	1b=Tx output squelched for media lane 6	
	4	Tx5 Force Squelch	0b=No impact on Tx behavior for media lane 5	
			1b=Tx output squelched for media lane 5	_
	3	Tx4 Force Squelch	0b=No impact on Tx behavior for media lane 4	
	2	Ty2 Force Squaleb	1b=Tx output squelched for media lane 4	_
	2	Tx3 Force Squelch	0b=No impact on Tx behavior for media lane 3 1b=Tx output squelched for media lane 3	
	1	Tx2 Force Squelch	0b=No impact on Tx behavior for media lane 2	-
	1	TAZ Force oquelen	1b=Tx output squelched for media lane 2	
	0	Tx1 Force Squelch	0b=No impact on Tx behavior for media lane 1	
			1b=Tx output squelched for media lane 1	
133	7:0	Reserved		RO
134	7	Tx8 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 8	RW
154	/	Txo Input Eq Adaptation Freeze	1b=Tx input eq adaptation frozen at last value for lane 8	Opt.
	6	Tx7 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 7	
		in input Eq Haaptadon Hotee	1b=Tx input eq adaptation frozen at last value for lane 7	
	5	Tx6 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 6	
			1b=Tx input eq adaptation frozen at last value for lane 6	
	4	Tx5 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 5	
		-	1b=Tx input eq adaptation frozen at last value for lane 5	_
	3	Tx4 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 4	
	2	To 2 Innut En Adaptation Engage	1b=Tx input eq adaptation frozen at last value for lane 4	_
	2	Tx3 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 3 1b=Tx input eq adaptation frozen at last value for lane 3	
	1	Tx2 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 2	_
	1	TX2 Input Eq Adaptation Treeze	1b=Tx input eq adaptation frozen at last value for lane 2	
	0	Tx1 Input Eq Adaptation Freeze	0b= No impact on Tx input eq adaptation behavior for lane 1	-
	-		1b=Tx input eq adaptation frozen at last value for lane 1	
135	7-6	Tx4 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location	WO
	5-4	Tx3 Input Eq Adaptation Store	00b=reserved	Opt.
	3-2	Tx2 Input Eq Adaptation Store	01b=store location 1	
	1-0	Tx1 Input Eq Adaptation Store	10b=store location 2	
			11b=reserved See section 6.2.4.4	
136	7-6	Tx8 Input Eq Adaptation Store	Tx Input Eq Adaptation Store location	wo
150	5-4	Tx7 Input Eq Adaptation Store	00b=reserved	Opt.
	3-2	Tx6 Input Eq Adaptation Store	01b=store location 1	opc.
	1-0	Tx5 Input Eq Adaptation Store	10b=store location 2	
			11b=reserved	
			See section 6.2.4.4	
137	7	Rx8 Polarity Flip	0b=No polarity flip for lane 8	RW
			1b=Rx output polarity flip for lane 8	Opt.
	6	Rx7 Polarity Flip	0b=No polarity flip for lane 7	
	5	Rx6 Polarity Flip	1b=Rx output polarity flip for lane 7 0b=No polarity flip for lane 6	_
	J		1b=Rx output polarity flip for lane 6	
	4	Rx5 Polarity Flip	0b=No polarity flip for lane 5	-
			1b=Rx output polarity flip for lane 5	
	3	Rx4 Polarity Flip	0b=No polarity flip for lane 4	
			1b=Rx output polarity flip for lane 4	
	2	Rx3 Polarity Flip	0b=No polarity flip for lane 3	7
			1b=Rx output polarity flip for lane 3	
	1	Rx2 Polarity Flip	0b=No polarity flip for lane 2	
			1b=Rx output polarity flip for lane 2	_
	0	Rx1 Polarity Flip	0b=No polarity flip for lane 1 1b=Rx output polarity flip for lane 1	
		1	I ID-KX OULDUL DOIARLY HID TOF IANG 1	1



138	7	Rx8 Output Disable	0b=Rx output enabled for lane 8	RW
			1b=Rx output disabled for lane 8	Opt.
	6	Rx7 Output Disable	0b=Rx output enabled for lane 7	
			1b=Rx output disabled for lane 7	
	5	Rx6 Output Disable	0b=Rx output enabled for lane 6	
			1b=Rx output disabled for lane 6	
	4	Rx5 Output Disable	0b=Rx output enabled for lane 5	
			1b=Rx output disabled for lane 5	
	3	Rx4 Output Disable	0b=Rx output enabled for lane 4	
			1b=Rx output disabled for lane 4	
	2	Rx3 Output Disable	0b=Rx output enabled for lane 3	
			1b=Rx output disabled for lane 3	
	1	Rx2 Output Disable	0b=Rx output enabled for lane 2	
			1b=Rx output disabled for lane 2	
	0	Rx1 Output Disable	0b=Rx output enabled for lane 1	
			1b=Rx output disabled for lane 1	
139	7	Rx8 Squelch Disable	0b=Rx output squelch permitted for lane 8	RW
			1b=Rx output squelch not permitted for lane 8	Opt.
	6	Rx7 Squelch Disable	0b=Rx output squelch permitted for lane 7	
			1b=Rx output squelch not permitted for lane 7	
	5	Rx6 Squelch Disable	0b=Rx output squelch permitted for lane 6	
			1b=Rx output squelch not permitted for lane 6	
	4	Rx5 Squelch Disable	0b=Rx output squelch permitted for lane 5	
			1b=Rx output squelch not permitted for lane 5	
	3	Rx4 Squelch Disable	0b=Rx output squelch permitted for lane 4	
			1b=Rx output squelch not permitted for lane 4	
	2	Rx3 Squelch Disable	0b=Rx output squelch permitted for lane 3	
			1b=Rx output squelch not permitted for lane 3	
	1	Rx2 Squelch Disable	0b=Rx output squelch permitted for lane 2	
			1b=Rx output squelch not permitted for lane 2	
Γ	0	Rx1 Squelch Disable	0b=Rx output squelch permitted for lane 1	
			1b=Rx output squelch not permitted for lane 1	

The optional controls follow this flow diagram.

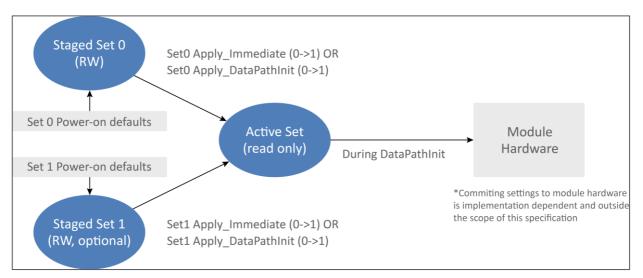


Figure 6: Control Set Data Flow Diagram



143	7	Staged Set 0 Lane 8 Apply_DataPathInit	1b=Apply Stag	ged Control Set 0 lane 8 settings using DataPathInit	WO RQD
	6	Staged Set 0 Lane 7 Apply_DataPathInit	1b=Apply Stag	ged Control Set 0 lane 7 settings using DataPathInit	
	5	Staged Set 0 Lane 6 Apply_DataPathInit	1b=Apply Stag	ged Control Set 0 lane 6 settings using DataPathInit	
-	4	Staged Set 0 Lane 5	1b=Apply Stag	ged Control Set 0 lane 5 settings using DataPathInit	
-	3	Apply_DataPathInit Staged Set 0 Lane 4 Apply_DataPathInit	1b=Apply Stag	ged Control Set 0 lane 4 settings using DataPathInit	-
	2	Staged Set 0 Lane 3 Apply_DataPathInit	1b=Apply Stag	ged Control Set 0 lane 3 settings using DataPathInit	
-	1	Staged Set 0 Lane 2 Apply_DataPathInit	1b=Apply Stag	ged Control Set 0 lane 2 settings using DataPathInit	
	0	Staged Set 0 Lane 1 Apply_DataPathInit	1b=Apply Stag	ged Control Set 0 lane 1 settings using DataPathInit	
144	7	Staged Set 0 Lane 8 Apply_Immediate	1b=Apply Stag State transitio	ged Control Set 0 lane 8 settings with no Data Path ns	WO RQD
	6	Staged Set 0 Lane 7 Apply_Immediate	1b=Apply State State transitio	ged Control Set 0 lane 7 settings with no Data Path ns	
	5	Staged Set 0 Lane 6 Apply_Immediate	State transitio		
-	4	Staged Set 0 Lane 5 Apply_Immediate	State transitio		
	3	Staged Set 0 Lane 4 Apply_Immediate	State transitio		
	2	Staged Set 0 Lane 3 Apply_Immediate	State transitio		
	1	Staged Set 0 Lane 2 Apply_Immediate	State transitio		
	0	Staged Set 0 Lane 1 Apply_Immediate	State transitio	ged Control Set 0 lane 1 settings with no Data Path ns	
145	7-4	Staged Set 0 Lane 1 Ap		ApSel code from Table 8-13 or Table 8-39, lane 1	RW
	3-1	Staged Set 0 Lane 1 Da		First lane of the data path containing lane 1 000b=Lane 1, 001b=Lane 2, etc.	RQD
	0	Staged Set 0 Lane 1 Ex	-	0b=Use Application-defined settings for lane 1 1b=use Staged Set 0 control values for lane 1	
146	7-4	Staged Set 0 Lane 2 Ap		ApSel code from Table 8-13 or Table 8-39, lane 2	RW
	3-1	Staged Set 0 Lane 2 Data Path ID		First lane of the data path containing lane 2 000b=Lane 1, 001b=Lane 2	RQD
	0	Staged Set 0 Lane 2 Explicit Control		0b=Use Application-defined settings for lane 2 1b=use Staged Set 0 control values for lane 2	
147	7-4	Staged Set 0 Lane 3 Ap		ApSel code from Table 8-13 or Table 8-39, lane 3	RW
-	3-1	Staged Set 0 Lane 3 Da		First lane of the data path containing lane 3 000b=Lane 1, 001b=Lane 2, etc.	RQD
1.0	0	Staged Set 0 Lane 3 Ex	-	0b=Use Application-defined settings for lane 3 1b=use Staged Set 0 control values for lane 3	
148	7-4 3-1	Staged Set 0 Lane 4 Ap Staged Set 0 Lane 4 Da		ApSel code from Table 8-13 or Table 8-39, lane 4 First lane of the data path containing lane 4	RW RQD
-	0	Staged Set 0 Lane 4 Ex	plicit Control	000b=Lane 1, 001b=Lane 2, etc. 0b=Use Application-defined settings for lane 4 1b=use Staged Set 0 control values for lane 4	-
149	7-4	Staged Set 0 Lane 5 Ap	Sel code	ApSel code from Table 8-13 or Table 8-39, lane 5	RW
112	3-1	Staged Set 0 Lane 5 Da		First lane of the data path containing lane 5 000b=Lane 1, 001b=Lane 2, etc.	RQD
	0	Staged Set 0 Lane 5 Ex	plicit Control	0b=Use Application-defined settings for lane 5 1b=use Staged Set 0 control values for lane 5	1
150	7-4	Staged Set 0 Lane 6 Ap	Sel code	ApSel code from Table 8-13 or Table 8-39, lane 6	RW
	3-1	Staged Set 0 Lane 6 Da		First lane of the data path containing lane 6 000b=Lane 1, 001b=Lane 2, etc.	RQD
-	0	Staged Set 0 Lane 6 Ex	plicit Control	0b=Use Application-defined settings for lane 6 1b=use Staged Set 0 control values for lane 6	1



151	7-4	Staged Set 0 Lane 7 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 7	RW
	3-1	Staged Set 0 Lane 7 Data Path ID	First lane of the data path containing lane 7	RQD
			000b=Lane 1, 001b=Lane 2, etc.	
ľ	0	Staged Set 0 Lane 7 Explicit Control	0b=Use Application-defined settings for lane 7	
			1b=use Staged Set 0 control values for lane 7	
152	7-4	Staged Set 0 Lane 8 ApSel code	ApSel code from Table 8-13 or Table 8-39, lane 8	RW
l l	3-1	Staged Set 0 Lane 8 Data Path ID	First lane of the data path containing lane 8	RQD
			000b=Lane 1, 001b=Lane 2, etc.	
ŀ	0	Staged Set 0 Lane 8 Explicit Control	0b=Use Application default settings for lane 8	
			1b=use Staged Set 0 control values for lane 8	
153	7	Staged Set 0 Tx8	1b=Enable	RW
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	Req
ľ	6	Staged Set 0 Tx7	1b=Enable	- ·
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	5	Staged Set 0 Tx6	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	4	Staged Set 0 Tx5	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
Γ	3	Staged Set 0 Tx4	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
[2	Staged Set 0 Tx3	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
[1	Staged Set 0 Tx2	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
	0	Staged Set 0 Tx1	1b=Enable	
		Adaptive Input Eq Enable	0b=Disable (use manual fixed EQ)	
154	7-6	Staged Set 0 Tx4	Recall stored Tx Eq adaptation value,	RW
		Adaptive Input Eq Recall	00b=do not Recall	Req
	5-4	Staged Set 0 Tx3	01b=store location 1	
ļ		Adaptive Input Eq Recall	10b=store location 2	
	3-2	Staged Set 0 Tx2	11b=reserved	
		Adaptive Input Eq Recall	See section 6.2.4.4 for Store/Recall methodology	
	1-0	Staged Set 0 Tx1		
		Adaptive Input Eq Recall		
155	7-6	Staged Set 0 Tx8	Recall stored Tx Eq adaptation value,	RW
-		Adaptive Input Eq Recall	00b=do not Recall	Req
	5-4	Staged Set 0 Tx7	01b=store location 1	
-		Adaptive Input Eq Recall	10b=store location 2	
	3-2	Staged Set 0 Tx6	11b=reserved	
		Adaptive Input Eq Recall	See section 6.2.4.4 for Store/Recall methodology	
	1-0	Staged Set 0 Tx5		
		Adaptive Input Eq Recall		
156	7-4	Staged Set 0 Tx2 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx1 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
157	7-4	Staged Set 0 Tx4 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx3 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
158	7-4	Staged Set 0 Tx6 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
	3-0	Staged Set 0 Tx5 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
159	7-4	Staged Set 0 Tx8 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	RW
1.50	3-0	Staged Set 0 Tx7 Input Eq control	Manual fixed Tx input eq control (See Table 6-4)	Req
160	7	Staged Set 0 Tx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW
ŀ	6	Staged Set 0 Tx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	Req
ļ	5	Staged Set 0 Tx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	_
ļ	4	Staged Set 0 Tx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	_
ļ	3	Staged Set 0 Tx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	_
ļ	2	Staged Set 0 Tx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	_
Ļ	1	Staged Set 0 Tx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	_
	0	Staged Set 0 Tx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	

161	7	Staged Set 0 Rx8 CDR control	1b=CDR enabled, 0b=CDR bypassed	RW
	6	Staged Set 0 Rx7 CDR control	1b=CDR enabled, 0b=CDR bypassed	Opt.
	5	Staged Set 0 Rx6 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	4	Staged Set 0 Rx5 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	3	Staged Set 0 Rx4 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	2	Staged Set 0 Rx3 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	1	Staged Set 0 Rx2 CDR control	1b=CDR enabled, 0b=CDR bypassed	
	0	Staged Set 0 Rx1 CDR control	1b=CDR enabled, 0b=CDR bypassed	
162	7-4	Staged Set 0 Rx2 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx1 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
163	7-4	Staged Set 0 Rx4 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx3 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
164	7-4	Staged Set 0 Rx6 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx5 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
165	7-4	Staged Set 0 Rx8 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	RW
	3-0	Staged Set 0 Rx7 Output Eq control, pre-cursor	Rx output equalization pre-cursor ¹	Opt.
166	7-4	Staged Set 0 Rx2 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx1 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
167	7-4	Staged Set 0 Rx4 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx3 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
168	7-4	Staged Set 0 Rx6 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx5 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
169	7-4	Staged Set 0 Rx8 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	RW
	3-0	Staged Set 0 Rx7 Output Eq control, post-cursor	Rx output equalization post-cursor ¹	Opt.
170	7-4	Staged Set 0 Rx2 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx1 Output Amplitude control	Rx output amplitude ²	Opt.
171	7-4	Staged Set 0 Rx4 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx3 Output Amplitude control	Rx output amplitude ²	Opt.
172	7-4	Staged Set 0 Rx6 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx5 Output Amplitude control	Rx output amplitude ²	Opt.
173	7-4	Staged Set 0 Rx8 Output Amplitude control	Rx output amplitude ²	RW
	3-0	Staged Set 0 Rx7 Output Amplitude control	Rx output amplitude ²	Opt.

4.4 Low Speed Signals

This tab allows to control and monitor the HW signals, depending on the selected device. The sections below define the control signals for each group of devices that share the same HW signals, separately.

4.4.1 QDD Family

This family includes MCBs like ML4062-MCB, ML4062-MCB-MXP and ML4062-TR.

Module Input signals:

LPMode:

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

ResetL:

- If set to Low: Module is in Reset state
- If set to High: Module is out of Reset state

ModSelL:

- If set to Low: Module is selected and I2C communication is active
- If set to High: Module is not selected and I2C communication is inactive



Module Output signals:

IntL:

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present

ModPrsL:

- If Read Low: Module is physically present
- If Read High: Module is physically absent

Get button is used to read the current state of these signals.

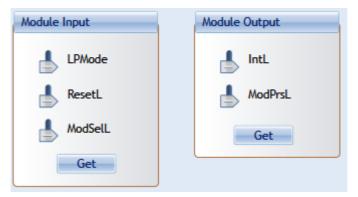


Figure 7: QDD HW Signals

4.4.2 OSFP Family

This family includes MCBs like ML4064-MCB, ML4064-TR.

Module Input signals:

LPWn:

- If set to Low: Module is in Low Power Mode
- If set to High: Module is in High Power Mode

RSTn:

- If set to Low: Module is in Reset State
- If set to High: Module is out of Reset State

Module Output signals:

PRSn:

- If Read Low: Module is physically present
- If Read High: Module is physically absent

INT:

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present



Module Input	Module Output
LPWn	PRSn
RSTn	
Get	Get

Figure 8: OSFP HW Signals

4.4.3 DSFP Family

The DSFP family includes the ML4019-MCB board.

The control signals of this family are similar to those in OSPF. Refer to section 5.4.2 for more details.

4.4.4 QSFP Family

This includes MCB like ML4041K.

Module Input signals:

LPMode:

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

ResetL:

- If set to Low: Module is in Reset state
- If set to High: Module is out of Reset state

ModSelL:

- If set to Low: Module is selected and I2C communication is active
- If set to High: Module is not selected and I2C communication is inactive

Module Output signals:

IntL:

- If Read Low: interrupt source is present
- If Read High: no interrupt source is present

ModPrsL:

- If Read Low: Module is physically present
- If Read High: Module is physically absent

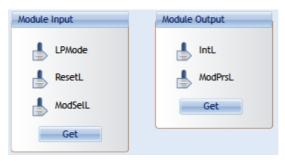


Figure 9: QSFP HW Signals



4.4.5 SFP-DD Family

This includes MCB like ML4022-MCB.

Module Input signals:

LPMode:

- If set to Low: Module is in High Power Mode
- If set to High: Module is in Low Power Mode

TxDisable0/ TxDisable1:

Set to Low or High by the user for CH0 and CH1 respectively

Module Output signals:

TxFault0/TxFault1:

Output state (Low or High) from the Module for CH0 and CH1 respectively

RXLOS0/RXLOS1:

Output state (Low or High) from the Module for CH0 and CH1 respectively

User should click on **Refresh** button to get the current output signals state.

Rate Select HW Control Contacts:

Speed0-1/ Speed 1-1:

Set the rate of the Receiver for CH0 and CH1 respectively

Speed0-2/ Speed 1-2:

• Set the rate of the Transmitter for CH0 and CH1 respectively

Reserved Pins:

RSVD / RSVD2:

- As Output: pins are set to High or Low
- As Input: Pins are Tri-stated

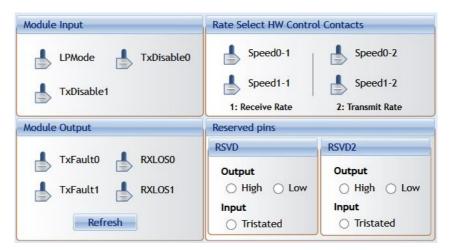


Figure 10: SFP-DD HW Signals



4.5 Identification

The Identification tab summarizes module specifications, vendor information and others.

Controls Low Speed Signals Identification	Options Available			
Refresh Page		Cable Length		
		Single Mode Fiber		
Specifications		Length (OM5)		
Identifier		Length (OM4)		
Power Class		Length (OM3 50µm)		
CLEI		Length (OM2 50 µm)		
Connector type		Length (Copper)		
Device Technology		Vendor		
Wavelength		Name		
Wavelength Tol.		oui		
Max Case Power		Part Number		
Wavelength control		Revision		
Cooling		Serial Number		
Tunable		Date Code		
·		Lot Code		
		Vendor Specific		

Figure 11: Identification Tab

The following table shows the corresponding ID registers, along with their names and description.

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power	
		characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	



4.6 Options Available

This tab specifies the options implemented in the module.

Monitor					Options Availat	Load/Save MSA		
	Click	to refresh this ;	page	Refresh				
	Exte	nded Ethernet	Compliance Codes:					
		Rx Optical Pov	ver Measurement Type	:		Rx CDR Loss of Lock (LC	L) Flag implemented	
		Rx output amp	olitude implemented			Rx Loss of Signal impler	nented	
		Tx Squelch im	plemented			Rx Optical Power Monito	or implemented	
		Tx Force Sque	lch implemented			Tx Optical Power Chann	el Monitoring implemented	
		Tx Squelch Dis	able Implemented			Tx Bias Monitor implem	ented	
		Tx Disable im	plemented			Tx adaptive Equalizatio	n implemented	
		Tx polarity fli	p implemented		\bigcirc	Tx input Equalization in	plemented	
		Rx Squelch Di	sable implemented			Tx CDR Bypass impleme	nted	
		Rx Output Dis	able implemented			Tx CDR implemented		
		Rx polarity fli	ip implemented			Staged Set 1 implement	ed	
		Tx CDR Loss o	of Lock (LOL) Flag imp	lemented		Rx Output Control imple	emented	
		Tx LOS Flag ir	mplemented			Rx CDR Bypass impleme	ented	
		Tx Fault Flag	implemented			Rx CDR implemented		

Figure 12: Options Available Tab

The following table shows the corresponding registers, along with their names and description.

RO
RQD
1
1
10
S



152	7-0	Per lane CDR Power saved	place	mum power consumption saved per CDR per lane when ed in CDR bypass in multiples of 0.01 W rounded up to the whole multiple of 0.01 W	RO Opt.	
153	7	Rx Output Amplitude code 0011b implemented ¹		=Amplitude code 0011b not implemented =Amplitude code 0011b implemented		
	6	Rx Output Amplitude code 0010b implemented ¹		p=Amplitude code 0010b not implemented p=Amplitude code 0010b implemented		
	5	Rx Output Amplitude code 0001b implemented ¹	0b=/	Amplitude code 0001b not implemented Amplitude code 0001b implemented	1	
	4	Rx Output Amplitude code 0000b implemented ¹	0b=/	Amplitude code 0000b not implemented Amplitude code 0000b implemented	1	
	3-0	Max Tx Input Eq	Maxi	imum supported value of the nput Equalization control for manual/fixed programming.	1	
154	7-4	Max Rx Output Eq	(see	section 6.2.4.1) imum supported value of the	RO	
134	3-0	Post-cursor Max Rx Output Eq Pre-	Rx O	Output Eq Post-cursor control. (see section 6.2.4.2)	Opt.	
		cursor Rx Output Eq Pre-cursor control (see section 6.2.4.2)				
Byte	Bit	Name		Description	Туре	
155	7	Wavelength control impleme	ented	0b=No wavelength control 1b=Active wavelength control implemented	RO RQD	
	6	Tunable transmitter implemented		0b=Transmitter not tunable 1b=Transmitter tunable (page 04h and bank page 12h shall be implemented)		
	5-4	Tx Squelch implemented		00b=Tx Squelch not implemented 01b=Tx Squelch reduces OMA 10b=Tx Squelch reduces Pave		
				11b=User control, both OMA and Pave squelch supported. (see Table 8-7)		
	3	Tx Force Squelch implemented		0b=Tx Force Squelch not implemented 1b=Tx Force Squelch implemented		
	2	Tx Squelch Disable implemented		0b=Tx Squelch Disable not implemented		
Byte	Bit	Name		Description		
				1b=Tx Squelch Disable implemented	_	
	1	Tx Disable implemented		0b=Tx Disable not implemented 1b=Tx Disable implemented		
				Ob-Ty Delarity Elip pet implemented		
156	0	Tx Polarity Flip implemented	l	0b=Tx Polarity Flip not implemented 1b=Tx Polarity Flip implemented		
156	7-3	Tx Polarity Flip implemented Reserved			RO ROD	
156	-	· · ·		1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented	RO RQD RO RQD	
156	7-3	Reserved		1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented	RQD RO	
156	7-3 2	Reserved Rx Squelch Disable impleme	nted	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented	RQD RO	
156	7-3 2 1	Reserved Rx Squelch Disable impleme Rx Disable implemented	nted	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented	RQD RO RQD RO	
	7-3 2 1 0	Reserved Rx Squelch Disable impleme Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented	nted I	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented	RQD RO RQD	
	7-3 2 1 0 7-4	Reserved Rx Squelch Disable impleme Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl	nted I	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx CDR Loss of Lock flag not implemented	RQD RQD RQD RO RQD RO	
	7-3 2 1 0 7-4 3	Reserved Rx Squelch Disable impleme Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented	nted I	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx Loss of Signal flag not implemented	RQD RQD RQD RO RQD RO	
	7-3 2 1 0 7-4 3 2	Reserved Rx Squelch Disable impleme Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented	I I Iag	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx Loss of Signal flag not implemented 0b=Tx Loss of Signal flag not implemented 0b=Tx Fault flag not implemented	RQD RQD RQD RO RQD RO	
	7-3 2 1 0 7-4 3 2 1	Reserved Rx Squelch Disable impleme Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented	I I Iag	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx Loss of Signal flag not implemented 1b=Tx Loss of Signal flag implemented	RQD RQ RQD RQ RQ RQ RQ RQ RQ RQ RQ	
157	7-3 2 1 0 7-4 3 2 1 0	Reserved Rx Squelch Disable impleme Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented Tx Fault flag implemented	I I Iag	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx Loss of Signal flag not implemented 0b=Tx Loss of Signal flag not implemented 0b=Tx Fault flag not implemented	RQD RQ RQD RQ RQD RQ RQD	
157	7-3 2 1 0 7-4 3 2 1 0 7-3	Reserved Rx Squelch Disable impleme Rx Disable implemented Rx Polarity Flip implemented Reserved Tx Adaptive Input Eq Failfl implemented Tx CDR LOL flag implemented Tx LOS flag implemented Reserved	I I Iag	1b=Tx Polarity Flip implemented 0b=Rx Squelch Disable not implemented 1b=Rx Squelch Disable implemented 0b=Rx Disable not implemented 1b=Rx Disable implemented 0b=Rx Polarity Flip not implemented 1b=Rx Polarity Flip implemented 0b=Tx Adaptive Input Eq Fail flag not implemented 1b=Tx Adaptive Input Eq Fail flag implemented 0b=Tx CDR Loss of Lock flag not implemented 1b=Tx Loss of Signal flag implemented 0b=Tx Fault flag not implemented 0b=Tx Fault flag not implemented 0b=Tx Fault flag not implemented 0b=Tx CDR Loss of Lock flag not implemented 0b=Tx Loss of Signal flag implemented 0b=Tx Fault flag not implemented 0b=Tx Fault flag not implemented 0b=Tx CDR Loss of Lock flag not implemented 0b=Rx CDR Loss of Lock flag not implemented	RQD RQ RQD RQD RQ RQD RQ RQD RQ RQD RO RQD RO	

multiLane	

Byte	Bit	Name	Description	Туре
159	7-6	Reserved		RO
				RQD
	5	Custom monitor implemented	0b=Custom monitor not implemented	RO
			1b=Custom monitor implemented	RQD
	4	Aux 3 monitor implemented	0b=Aux 3 monitor not implemented	
			1b=Aux 3 monitor implemented	
	3	Aux 2 monitor implemented	0b=Aux 2 monitor not implemented	
			1b=Aux 2 monitor implemented	
	2	Aux 1 monitor implemented	0b=Aux 1 monitor not implemented	
			1b=Aux 1 monitor implemented	_
	1	Internal 3.3 Volts monitor	0b=Internal 3.3 V monitor not implemented	
	0	implemented	1b=Internal 3.3 V monitor implemented	_
	0	Temperature monitor implemented	0b=Temperature monitor not implemented	
160	7-5	Reserved	1b=Temperature monitor implemented	RO
100	4-3	Tx Bias current measurement	Multiplier for 2uA Bias current increment used in Tx Bias	RQD
	чJ	and threshold multiplier	current monitor and threshold registers (see Table 8-42	RQD
		and direction manapiler	and Table 8-62)	
			00b=multiply x1	
			01b=multiply x2	
			10b=multiply x4	
			11b=reserved	
	2	Rx Optical Input Power monitor	0b=Rx Optical Input Power monitor not implemented	
	-	implemented	1b=Rx Optical Input Power monitor implemented	
·	1	Tx Output Optical Power monitor	0b=Tx Output Optical Power monitor not implemented	
	-	implemented	1b=Tx Output Optical Power monitor implemented	
	0	Tx Bias monitor implemented	0b=Tx Bias monitor not implemented	
			1b=Tx Bias monitor implemented	
161	7	Reserved		RO
				RQD
	6-5	Tx Input Eq Store/Recall buffer	00b=Tx Input Eq Store/Recall not implemented	RO
		count	01b=Tx Input Eq Store/Recall buffer count=1	RQD
			10b=Tx Input Eq Store/Recall buffer count=2	
			11b=reserved	_
	4	Tx Input Eq Freeze implemented	0b=Tx Input Eq Freeze not implemented	
			1b=Tx Input Eq Freeze implemented	_
	3	Adaptive Tx Input Eq	0b=Adaptive Tx Input Eq not implemented	
	2	implemented	1b=Adaptive Tx Input Eq implemented	_
	2	Tx Input Eq fixed manual control	0b=Tx Input Eq Fixed Manual control not implemented	
		implemented	1b=Tx Input Eq Fixed Manual control implemented	_
	1	Tx CDR Bypass control implemented	0b=Tx CDR Bypass control not implemented (if CDR is implemented, it will be enabled)	
		Implemented	1b=Tx CDR Bypass control implemented	
	0	Tx CDR implemented	0b=Tx CDR not implemented	-
		TX CDX implemented	1b=Tx CDR implemented	
162	7-6	Reserved		RO
102				RQD
	5	Staged Set 1 implemented	Staged Control Set 1 implemented on Page 10h	RO
	4-3	Rx Output Eq control	00b=Rx Output Eq control not implemented	RQD
		implemented	01b=Rx Output Eq Pre-cursor control implemented	
			10b=Rx Output Eq Post-cursor control implemented	
			11b=Rx Output Eq Pre- and Post-cursor control	
			implemented	_
	2	Rx Output Amplitude control	0b=Rx Output Amplitude control not implemented	
		implemented	1b=Rx Output Amplitude control implemented	
	1	Rx CDR Bypass control	0b=Rx CDR Bypass control not implemented (if CDR is	
		implemented	implemented, it will be enabled)	
			1b=Rx CDR Bypass control implemented	
	0	Rx CDR implemented	0b=Rx CDR not implemented	
			1b=Rx CDR implemented	

4.7 Load/Save MSA

This tab allows the user to Load or Save his custom MSA configuration.

Data is displayed in a grid showing: register address, hex value, Decimal Values, ASCII value, MSA description.

Also the buttons available in this tab are summarized below:

- **Refresh Page**: Read MSA Registers, and refresh values.
- Write MSA to HW: Write the current MSA configuration to the module.
- Save MSA to file: Save the current MSA memory to a file using Comma separated values (CSV) format.
- Load MSA from file: Load MSA values from file and map it to MSA memory.
- Checksum for pages 00, 01 and 02

	Refresh Page		Write MSA to HW	- La	bad MSA from file Save MSA to file	
	Address	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description	
•	LowMem 0(00h)	0	0	0	ldentifier —	
	LowMem 1(01h)	0	0	0	Revision Compliance	Checksum (Page00 128-221)
	LowMem 2(02h)	0	0	0	CLEI code present	Stored
	LowMem 3(03h)	0	0	0	Module State	Calculated
<u> </u>	LowMem 4(04h)	0	0	0	Bank 0 flag summary	
	LowMem 5(05h)	0	0	0	Bank 1 flag summary	Checksum (Page01 130-254)
	LowMem 6(06h)	0	0	0	Bank 2 flag summary	Stored
	LowMem 7(07h)	0	0	0	Bank 3 flag summary	Calculated
	LowMem 8(08h)	0	0	0	Data Path/Module firmware fault and Module S	Calculated
	LowMem 9(09h)	0	0	0	Latched VCC3.3/Temp Alarm and Warning	Checksum (Page02 128-254)
	LowMem 10(0Ah)	0	0	0	Latched AUX1/2 Alarm and Warning	Stored
	LowMem 11(0Bh)	0	0	0	Latched Vendor Defined/AUX3 Alarm and Warn	
	LowMem 12(0Ch)	0	0	0	Reserved	Calculated
	LowMem 13(0Dh)	0	0	0	Custom	
	LowMem 14(0Eh)	0	0	0	Internally measured Temperature 1 MSB	
	LowMem 15(0Fh)	0	0	0	Internally measured Temperature 1 LSB	
	LowMem 16(10h)	0	0	0	Internally measured Supply 3.3v MSB	
	LowMem 17(11h)	0	0	0	Internally measured Supply 3.3v LSB	
	LowMem 18(12h)	0	0	0	Internally measured AUX1 MSB	
	LowMem 19(13h)	0	0	0	Internally measured AUX1 LSB	
	LowMem 20(14h)	0	0	0	Internally measured AUX2 MSB	

Figure 13: Load/Save MSA Tab

4.8 Load/Save Page 10/11h

This tab allows the user to Load or Save configuration for Page10h and Page11h. Data is displayed in a grid showing: register address, hex value, Decimal Values, ASCII value and MSA description. Buttons in this tab are described below:

- **Refresh Page**: Read Registers, and refresh values.
- Write MSA to HW: Write the current MSA configuration to the module.
- Save MSA to file: saves the current MSA memory to a file using Comma separated values (CSV) format.
- Load MSA from file: Loads MSA values from file and map it to MSA memory.



Refre	sh Page	Write	MSA to HW	Load MSA	from file Save MSA to file	
Addre	ss	Data(Hex)	Data(Dec.)	Data(Ascii)	MSA Description	-
Page16	(10h) 253(FDh)	0	0	0	Custom	
Page 10	(10h) 254(FEh)	0	0	0	Custom	
Page16	(10h) 255(FFh)	0	0	0	Custom	
Page 17	(11h) 128(80h)	0	0	0	Datapath State Encoding	
Page 17	(11h) 129(81h)	0	0	0	Datapath State Encoding	
Page 17	(11h) 130(82h)	0	0	0	Datapath State Encoding	
Page 17	(11h) 131(83h)	0	0	0	Datapath State Encoding	
Page 17	(11h) 132(84h)	0	0	0	Reserved	
Page 17	(11h) 133(85h)	0	0	0	Reserved	
Page 17	(11h) 134(86h)	0	0	0	Latched Data Path State Changed flag	
Page 17	(11h) 135(87h)	0	0	0	Latched Tx Fault flag	
Page 17	(11h) 136(88h)	0	0	0	Latched Tx LOS flag	
Page 17	(11h) 137(89h)	0	0	0	Latched Tx CDR LOL flag	
Page17	(11h) 138(8Ah)	0	0	0	Latched Tx Adaptive Input Eq. Fault	
Page 17	(11h) 139(8Bh)	0	0	0	Tx output power High Alarm	
Page 17	(11h) 140(8Ch)	0	0	0	Tx output power Low Alarm	
Page 17	(11h) 141(8Dh)	0	0	0	Tx output power High Warning	
Page 17	(11h) 142(8Eh)	0	0	0	Tx output power Low Warning	
Page 17	(11h) 143(8Fh)	0	0	0	Tx Bias High Alarm	

Load/Save Page 10/1

Figure 14: Load/Save Page 10/11h Tab

4.9 I2C R/W

This tab gives access to MSA registers.

- 1. Select the page in the **Memory Location**.
- 2. **Single Byte** window: to read/write one byte from the memory.
 - a. Address: The address to read/write from.
 - b. Memory Content: The data value read from or written to the selected address.

3. **Multi-bytes** window: to read multiple bytes between selected Starting Address and an End Address.

							I2C R/W		
nis page	Refrest	Page							
				Multip	le Bytes				
00 O Upper 03	Page 01(Optional) (Upper Page 02(Optic			End Addre (Decimal)	ss	Read	Save
er page number	Set			Add	ress Hex	Binary	ASCII		
Memory Cont (Hex)			ASCII	_					
Read	W	Irite							
	nis page 00 Upper 03 e above er page number Memory Con (Hex)	nis page Refrest 00 OUpper Page 01(Optional 03 e above er page number Set Memory Content Memor (Hex) (Binar	nis page Refresh Page 00 Upper Page 01(Optional) 03 e above er page number Set Memory Content (Hex) (Binary)	No. Refresh Page 00 Upper Page 01(Optional) Upper Page 02(Optional) 03 • above er page number Set Memory Content Memory Content ASCII (Hex) (Binary)	Nultip 00 Upper Page 01(Optional) Upper Page 02(Optional) 03 above er page number Set Memory Content Memory Content ASCII (Hex) (Binary)	Memory Content (Hex) Memory Content (Binary) ASCII	00 Upper Page 01(Optional) Upper Page 02(Optional) 03 above er page number Set Memory Content Memory Content (Hex) (Binary)	Nultiple Bytes 00 Upper Page 01(Optional) 03 above r page number Set Memory Content Memory Content Memory Content Memory Content Memory Content Memory Content	Nultiple Bytes 00 Upper Page 01(Optional) 03 Upper Page 02(Optional) 03 Clecimal) er page number Set Memory Content Memory Content Memory Content Memory Content Memory Content Memory Content ASCII Image: Clecimal (Clecimal)

Figure 15: I2C R/W Tab



4.10 QDD MXP

This tab is used only with ML4062-MCB-MXP.

The following tab allows the user to modify the DC Level within a range between 3.0 and 3.6, and to insert noise to the VCC by adding noise frequency between 0 and 12500000 Hz and control noise amplitude ranging from 0 to 120mV.

Two buttons are available under Noise Insertion Window:

- 1. Apply: this must be pressed so the noise frequency and amplitude take effect
- 2. Reset: this will set noise frequency and amplitude back to 0

									QDD MXP	
Th	us tab is on	ly avail:	able for ML40	162-MCB-W	YD					
		ly availa		J02-MCD-M	IVLE					
V	C				Noi	se Insertion				
					N	oise Frequency:	0 Hz			
							_			
	DC Level:		U	- 3.3 V	N	oise Amplitude:	V	0	mV	
							Apply	Reset		
								THE SEC		
										-
N.B	Press Enter each t	time you wri	te a value in a textbo	эх.						

Figure 16: QDD MXP Tab

4.11 I2C R/W Advanced

This tab gives access to MSA registers without specifying the Slave address.

- 1. Select Page Number under Memory Location window.
- 2. Under Single Byte window.
 - Write the corresponding Slave Address
 - o Write the Address to read from or write to
 - Data to be written to or Read from the selected address is under Memory Content field
- 3. Under Multi-Byte Read window.
 - o Write the corresponding Slave Address
 - o Select the Starting Address and the End Address to Read from



									I2C R/W Advanced
Mer	nory Location			Single Byte					
Pa	ge Number(Decimal	.)		Enter ASCII or	Hex or Binary				
0	0		Set	Slave Address	(Hex) Address(decimal) M	emory Content(Hex)	Memory Content(binary)	ASCII
						Read	Write		
				Multi-Byte Re	ad				
				Slave Address(Hex) Starting Ac (Decimal)	Idress End Ad			
							Read		
							Save		
				Address	Hex	Binary A	SCII		

Figure 17: I2C R/W Advanced Tab

4.12 Command Data Block (CDB) Message Communication

The Common Data Block (CDB) is a message communication protocol between the Host and a Module that allows the user to check and apply various settings on the interconnect, including updating the firmware. CDB is a Two Wire serial Interface (TWI) protocol based on the i2c for CMIS 4.0 and 5.0 between a Master (Initiator in 5.0) and Slave (Target in 5.0).

The host sends a CDB Command (CMD) message which is identified by a CMD ID and the module responds with a CDB Reply (REPLY) message without changing the CMD ID.

On the ML4062 Module Compliance Board (MCB), the CDB enables the issuing of commands from the MCB to the interconnect. The ML4062 MCB includes all CDB commands mentioned in CMIS 4.0 and CMIS 5.0.

 Monitor
 CDB
 Interrupt Masks
 Controls
 Low Speed Signals
 Identification
 Options Available
 Load/Sav

 Unlock CDB Feature
 CDB Commands
 CDB Feature and Capabilities Commands
 CDB Firmware Download Commands
 CDB Performance/Data Monitoring Commands
 CDB Performance/Data Monitoring Commands

 CDB License
 C:User:/User/Desktop
 License.tt
 Validate
 Validate

Unlock CDB feature by loading the purchased License File:

Figure 21: CDB License Validation



4.12.1 CDB Commands

- CMD 0000h Query Status
- CMD 0001h Enter Password
- CMD 0002h Change Password
- CMD 0003h Enable/Disable Password Protection
- CMD 0004h General Abort
- CMD 0380h Loopbacks

		Detailed Map Registers			
Delay MSB (Dec) Delay LSB (Dec)		Name	Page (Hex)	Address (Hex)	Value (Hex)
0 0 Query	/ Status	CDB Status	00	25	01
		CDB Complete Flag	00	08	01
Password Entry/ Change (Dec)		Length of status	9F	88	03 1
	17	Unlock level and privileges	9F	89	00
0 0 16	17	Firmware download allowed	9F	8A	00
bort a CDB Command General Abort LPRBS BERT Loopbacks		nmand Progress			Export
ommand Progress					

Figure 22: CDB Commands

The CDB GUI includes detailed map registers that show what is returned by each command.

Here, for example, the query status command is being sent. A progress bar indicates the progress of the running CDB command. The GUI clearly indicates that the command was sent successfully (CDB status=1), that it asserts the CDB flag, and that it returns three bytes of data as shown with the corresponding value and description. The User can export this data (to an excel sheet) using the export button.

4.12.2 CDB Feature and Capabilities Commands

multiLane

- CMD 0040h Module Features: Identifies which commands are supported, from CMD 0 to CMD 00FF along with the maximum CDB command execution time.
- CMD 0042h Performance Monitoring: Identifies which commands are supported from 0200h to 02FFh.
- CMD 0043h Bert and diagnostics: Identifies CMD 0300h to 03FFh.
- CMD 0041h Read FW Features: Identifies many parameters supported the firmware features including firmware download transfer type, if copy/abort/full image readback commands are supported, start command payload size, erased byte, the firmware update features, if read/write firmware is supported, the firmware can be upgraded, etc. Use this feature to determine whether a device supports LPL or EPL firmware.

Command support 0 CMDs 0000h - 000Fh • • CMDs 0010h - 001Fh • CMDs 0020h - 002Fh •	3 4	7	Bert And Diag	C F	Name CDB Status CDB Complete Flag CDB flags Reserved CADs 0000h-0007h support	Page (Hex) 00 9F 9F	Address (Hex) 25 08 88 89	Value (Hex) 01 00 00	Description Success CDB Complete Flag Assertion Reserved for additional CDB flags
CMDs 0000h - 000Fh • • • CMDs 0010h - 001Fh • • CMDs 0020h - 002Fh • • CMDs 0030h - 003Fh • • CMDs 0030h - 004Fh • • CMDs 0050h - 005Fh • •		7	8 B 0000 0000 0000	C F	CDB Complete Flag CDB flags Reserved	00 9F	08 88	00 00	CDB Complete Flag Assertion
CMDs 0000h - 000Fh • • • • CMDs 0010h - 001Fh • • • CMDs 0010h - 001Fh • • CMDs 0020h - 002Fh • • CMDs 0030h - 003Fh • • CMDs 0040h - 004Fh • • CMDs 0050h - 005Fh • • • CMDs 0050h - 005Fh • • • • • CMDs 0050h - 005Fh • • • • • • • • • • • • • • • • • • •				0000	CDB flags Reserved	9F	88	00	
CMDs 0010h - 001Fh CMDs 0020h - 002Fh CMDs 0020h - 002Fh CMDs 0030h - 003Fh CMDs 0040h - 004Fh S CMDs 0040h - 004Fh CMDs 0050h - 005Fh CMDs 0050h - 005Fh				00000	Reserved	9F			
CMDs 0020h - 002Fh OCMDs 0030h - 003Fh OCMDs 0030h - 003Fh OCMDs 0040h - 004Fh OCMDs 0050h - 005Fh OCMDs 0				0000	CMDs 0000h-0007h support		9.4	00	Reserved
CMDs 0030h - 003Fh OCLAN CMDs 0040h - 004Fh OCLAN CMDs 0050h - 005Fh OCLAN				0000		9F	8A	07	Each bit represent a mask. If bit is "1
CMDs 0050h - 004Fh					CMDs 0008h-000Fh support		8B	00	Each bit represent a mask. If bit is "1
CMDs 0050h - 005Fh				0000	CMDs 0010h-0017h support		8C	00	Each bit represent a mask. If bit is "1
				0000	CMDs 0018h-001Fh support		8D	00	Each bit represent a mask. If bit is "1
CMDs 0060h - 006Fh				0000	CMDs 0020h-0027h support CMDs 0028h-002Fh support		8E 8F	00	Each bit represent a mask. If bit is "1 Each bit represent a mask. If bit is "1
	00 00			0000	CMDs 0028h-002Fh support CMDs 0030h-0037h support		90	00	Each bit represent a mask. If bit is "1
CMDs 0070h - 007Fh				0000	CMDs 0038h-003Fh support		91	00	Each bit represent a mask. If bit is "1 -
CMDs 0080h - 008Fh 001				00000	•			1.00	
				0000					Export
CMDs 0090h - 009Fh 🔘 🔘	00 00			0000					Export
CMDs 00A0h - 00AFh				0000					
CMDs 00B0h - 00BFh 🔘 🔘				0000	Command Progress				
CMDs 00C0h - 00CFh 🔘 🔘				0000					
CMDs 00D0h - 00DFh				0000	Success	_			
CMDs 00E0h - 00EFh	00 00			0000	5000033				
				0000	L				
CMDs 00F0h - 00FFh 🔿 🔿				0000					

Figure 23: CDB Feature and Capabilities Commands

The green buttons indicate which commands are supported. In this case, the module feature command is returning the corresponding data in the detailed map register and indicates that CMDs 0,1,2,40,41,42,43 are supported (other modules might support other commands).

4.12.3 CDB Firmware Download Commands

- CMD 0101h, 0103h, 0107h Program LPL: Loads the firmware binary file for Local Payload (LPL). Allows for updating interconnect firmware.
- CMD 0101h, 0104h, 0107h Program EPL: Loads the firmware binary file for Extended Payload (EPL). EPL support varies depending on the interconnect. Allows for updating interconnect firmware.
- CMD 0101h, 0105h, 0107h Read Image LPL: Read the latest upgraded firmware image using LPL



- Export Image: Exports an image of the firmware after the read is completed as a .bin file, which in turn can be loaded into and read by other interconnects.
- CMD 0102h Abort FW download: Stops the firmware from being installed onto the interconnect.
- **CMD 0109h Run image**: After the new LPL or EPL Firmware is loaded, this command switches to the latest firmware image. Does not replace the existing firmware image on the interconnect.
- CMD 010Ah Commit image: Replaces the firmware image on the interconnect with the new loaded firmware image. Prior to this command being executed, the old firmware will still be executed on startup. Always ensure the new image is running perfectly (by running it on the interconnect using the previous commands) before using this command.
- CMD 0108h Copy image A to B/B to A: In the event of two images being present on the same interconnect and both images are written to flash, this command makes ensures that both images are identical, with the copied image being specified in the commands as either image A to image B, or image B to image A.
- CMD 0100h Get FW Info: Loads the information about the latest firmware on the interconnect, for both image A and image B.

CDB Firmware Download Commands	Get Firmwar	e Info			
Load corresponding binary file	- Get FW I	nfo			
C:\Users\User\Desktop \400GSR8_034ATN_SOFT_V130T01_CDB.bin			J		
	CDB Detailed	Map Registers			
	Name	Page (Hex)	Address (Hex)	alue (Hex)	Description
Download new firmware image	CDB Stat				Success
Program LPL Program EPL		plete Flag 00	08 0		CDB Complete Flag Assertion
		e Status Flags 9F	88 0		Bitmask to indicate FW Status.00h: Fa
Read latest downloaded firmware image	Informat		89 0		Bit 0: Firmware image A is present in
	Image A		8A 0		Image A Major revision
Read Image LPL Read Image EPL Export Image	Image A		8B 0		Image A Minor revision
	Image A		8C 0		Image A Build number
Abort firmware download	Image A		8D 0		Image A Build number
		Extra String 9F	8E 0		Image A Extra String Image A Extra String
Abort Firmware		Extra String 9F Extra String 9F	8F 0		Image A Extra String
		Extra String 9F	91 0		Image A Extra String
Run downloaded firmware image	intage A	Extra Suring 9F	91 0	0	image A Extra String
Delay MSB (Dec) Delay LSB (Dec) Reset					
0 •					Export
Run Image	Image				
Attempt Hitless Reset to Inactiv	Command Pr	ogress			
Switch to the new firmware image Traffic affecting Reset to Runnin	Image				
Commit Image Attempt Hitless Reset to Runnin	Image Success				

Figure 24: CDB Firmware Download Commands

4.12.4 CDB Performance/Data Monitoring Commands

CMD 0200h PM Controls: Extract Performance Monitoring data records such as minimum/average/maximum values. "No Operation" reads the most recent values, while "Clear All" clears the extracted values for all lanes in the interconnect.



- **CMD 0280h Data Monitoring and Recording Controls**: "Refresh" loads the most recent attributes. "Clear All" clears all values for all parameters for all lanes at the same time.
- CMD 0281h Data monitoring and recording advertisement

- **CMD 0290h Temperature Histogram**: Displays the temperature intervals of the interconnect and how long it stayed at each temperature interval.
- CMD 0210h, 0211h Get Module PM LPL/EPL: Choose parameters of the module's performance monitoring records, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- CMD 0212h, 0213h Get PM Host Side LPL/EPL: Choose parameters of the host's performance monitoring records, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- CMD 0214h, 0214h Get PM Media Side LPL/EPL: Choose parameters the performance monitoring records of specific lanes, and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.
- CMD 0216h, 0217h Get Data Path PM LPL/EPL: Choose the data path for specific lanes and replace the current values of the minimum, average, and maximum values. "Refresh" replaces the old values, while "Clear and Read" reads and resets the old values.

	upt Masks CDB							
						CDB Perform	nance/Data Monitoring Co	ommands
CDB Performance/Data Monitoring	Get PM Host Side LPL/EPL		Get	PM Media Side LPL/EPL				
PM Controls	Host Side Lane SNR			Media Side Lane SNR	Return 6-byte PM 🔹	Record Type		
PM Objects are In 👻 Link mode	Host Side PAM4 LTP			Media Side PAM4 LTP		Lane 1-8	Refresh and Read LPL	
No Operation Clear all PM Feature Information	Return 8-byte PM · Re			Tx Laser Bias		Lane 9-16	Clear and Read LPL	
Read PM Additional Features	Recurit orbyce PM	Lane 1-8		Tx Power		Lane 17-24	Clear and Read EPL	
Data Monitoring and Recording Controls				Rx Power		Lane 25-32	Refresh and Read EPL	
Refresh Clear		Lane 9-16		Per-Lane Laser Temperat	ure			
DM and Recording Advertisement		Lane 17-24		0				
DM Advertisement		Lane 25-32	CDB	Detailed Map Registers				
Temperature Histogram	Refresh and Read LPL	Clear and Read LPL		Name	Page (He	ex) Address	(Hex) Value (Hex)
 Save Current histogram to NVR Return histogram 	Refresh and Read EPL	Clear and Read EPL	<u>۲</u>	CDB Status	00	25	41	
Clear Temperature histogram				CDB Complete Flag	g 00	08	00	
Temperature Histogram			•					_
Get Module PM LPL/EPL	Get Data Path PM LPL/EPL							
Return 6-byte PM - Record Type	Frame Error Count							
Module Temperature	Media Side Pre-FEC 8							
Vcc	- R	ecord Type						
Aux1		Data Path Lane 1-8	•					<u> </u>
Aux2		Data Path Lane 9-16					Exp	ort
Refresh and Read LPL		Data Path Lane 17-24	Com	mand Progress				
Clear and Read LPL		Data Path Lane 25-32	_					
Refresh and Read EPL	Refresh and Read LPL	Refresh and Read EPL	Exect	ution Failed				
Clear and Read EPL	Clear and Read LPL	Clear and Read EPL						

Figure 25: CDB Performance/Data monitoring Commands



Software Revision

V2.2.1: latest Software Revision, which this document is based on.