

ML4039B

Technical Reference

200G Bit Error Ratio Tester



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1. General Description

The ML4039B is a fully featured 200G BERT that can be configured as a 4x26.5625 GBaud BERT. NRZ and PAM4 modes are supported at both low and high rates. It is used in Production testing of transceivers as for Functional and SI testing.

The ML4039B is designed for 200G applications. This instrument is a fully integrated, ultra-compact, USB/Fast Ethernet controlled instrument that combines all the functions and features of a signal generator, bit error-ratio tester and data analysis system with Post-Emphasis and Pre-Emphasis, 7 taps FIR and CTLE capabilities.

2. Ordering information

The ML4039B can be ordered with the following part number.

ML4039B	4 channel BERT
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Table 1: Hardware ordering information

For more details please refer to the below link:

<https://multilaneinc.com/product/ml4039b-2/>

3. Operating conditions

A 110/220V adapter is used to power-up the board.

If the temperature of the board inside the box has surpassed the 70°C value, in order to prevent overheating, this temperature is considered as the cutoff value.

The instrument will resume normal functionality again once the temperature is within the optimal range.

4. Block Diagram

The ML4039B block diagram is illustrated in figure 1. Signals are transmitted from the TX side through four independent channels, and the received signals are routed from the RX side of the error detector. These signals can be monitored and controlled channel by channel.

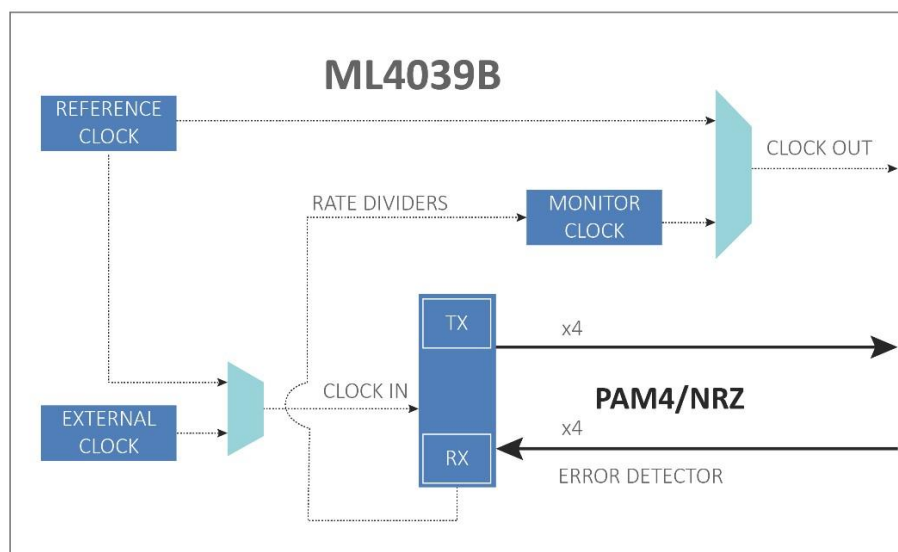


Figure 1: ML4039B block diagram

5. Hardware design overview

Figure 2 shows a general view of the ML4039B.



Figure 2: ML4039B

The instrument dimensions are shown in figures 3 and 4.



Figure 3: ML4039B front view with dimensions

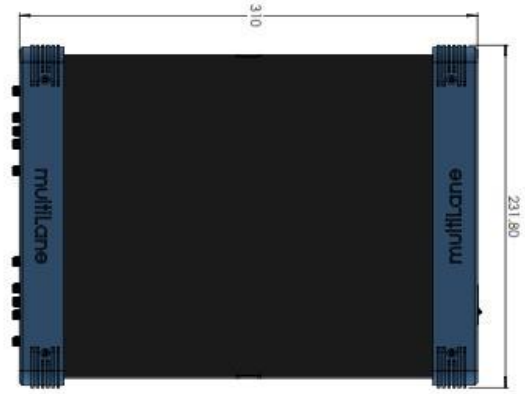


Figure 4: ML4039B top view with dimensions

With an overall weight of two kilograms.

The back plate includes an ON-OFF switch button, Ethernet and USB ports. A 110/220V power adapter can be connected to supply the board with the required power.

The faceplate shows two SMA connectors for clock connection: clock-in and clock-out. And a push button to turn on/ off the instrument.

The faceplate includes a push button, an LCD screen that shows the RX lock status, BER and SNR values on each channel, temperature value, also displays IP and firmware version.

Once powered up, the switch and push buttons turned on, the board should be able to perform all the required measurements.

6. Clock Configuration

The ML4039B supports input and output clocks. For the Clock out: The user can switch between two options: reference clock and monitor clock.

The monitor clock supports up to 800MHz differential clock rate. In order to get an optimal eye using the monitor clock, Ch1 should be set in loopback mode and lock, as it will be considered as the CDR that the ML4039B will use to generate the Monitor clock. The rate dividers are: 32, 64, 128, 256, 512, 1024, 2048, and 4096. For lower jitter values, it is required to use any adjacent channel as a trigger.

The reference clock supports up to 425 MHz with an optimal value of 156.25MHz.

The analog clock input range varies between 80-700 MHz with an optimal value of 156.25MHz.

7. Transmitter side characteristics

As described above the TX signals are transmitted through four independent channels. The Low/ High voltage settings for each channel, generated during the calibration process, are being applied on high or low rates, and in both eye modes: NRZ and PAM4. These settings, once applied and saved, ensure that ML4039B performs all the required measurements.

These settings can be controlled by the user in advanced mode.

In this way the user can control all the TX settings including: TX pattern, amplitude, the 3 FFE taps: Pre-emphasis, Main Tap, Post-Emphasis or the 7 FIR taps... The Outer and Inner level of the PAM4 eye can be adjusted in advanced mode.

The ML4039B operates in PAM4 and NRZ modes, on numerous bitrates.

The BERT locks on all the supported rates, amplitudes and patterns. The parameters are mentioned in table 2.

The TX Equalization is a digital combination of FFE and DFE, PAM4 gray coding. Test pattern generator per lane includes error injection.

The patterns, error insertion and emphasis taps can be checked and controlled per lane.

Kindly refer to the user manual paragraph 11 for more details to operate the ML4039B

Table 2 shows the TX Output Characteristics of the ML4039B.

Parameter			Typical	Maximum	Unit
Line Rate	NRZ		1.12 -1.56 2.24 -6.1 6.5 -29	up to 29	Gbps
	PAM4		6.5 -29	up to 29	Gbaud
Clock-out Amplitude			TBD		mV
Clock-out Frequency	Monitor		Rate/4096 – Rate/32	~ 900	MHz
	Reference		156.25	161.11	
Output Amplitude	Low Rate (NRZ & PAM4)	Advanced Mode	Up to 550		mV
		Low voltage settings Mode	Up to 460		
	High Rate (NRZ & PAM4)	Advanced Mode	Up to 480		
		Low voltage settings Mode	Up to 370		
Patterns			PRBS 7/9/11/13/15/23/31 /58/9_4, JP03B, IEEE 802.3bs, OIF-CEI-3.1, User defined		
Emphasis Resolution			± 1000		Steps

Table 2: TX output specifications

8. Receiver side characteristics

The receiver side characteristics are described in this section.

The BERT locks on different patterns, with the polarity inversion option. The equalizer can be tuned on a range of around 10 dB, the CTLE slider can be controlled channel by channel. Real-Time BER can be measured. Histograms and SNR shared across all four channels. Quadruple port CDR, being able to recover the supported rates.

Parameter		Typical	Maximum	Unit
Line Rate	NRZ	1.12 -1.56 2.24 -6.1 6.5 -29	up to 29	Gbps
	PAM4	6.5 -29	up to 29	Gbaud
Clock-in Amplitude		TBD		mV
Clock-in Frequency		156.25	80-700	MHz
Sensitivity	Low Rate	35		mV
	High Rate	40		
Patterns		PRBS 7/9/11/13/15/23/31		
CTLE			62	Steps

Table 3: Receiver specifications

9. Current revisions

The revision of the ML4039B is listed below:

All the listed features are tested using the following software and firmware:

- Software revision: MLBERT-GUI v.4.4.0.0
- Firmware revision: 4039B-RevD_LCD_V1_3

10. Future Features

The following features will be implemented in the future ML4039B versions:

- Calibrated CTLE slider

11. User Manual

11.1 GUI General Description

This section describes how to operate the ML4039B and all the capabilities of this BERT.

The product software is available on the company's website on the below link:

<https://multilaneinc.com/berts-gui/>

11.2 Installation

This chapter covers the installation of the instrument, addressing the following topics:

- System Start-up
- How to connect to the instrument

Note: For windows vista, 7, 8 and 10 users should always run the GUI as administrator.

First Steps

When the customer receives the instrument, it has a pre-configured IP address from the factory. This IP address is printed on a label on the instrument's back plate. The user can choose to keep this IP or to change it. If changing the IP is needed, there are two ways to do it: either through the USB interface, or through the Ethernet interface. If changing through USB is selected, then the USB driver of this instrument should be installed from the company's website, and the user needs to choose the application ETH config.

If the LAN interface is used to change the IP, then the user has to download the application "IPChanger" from the company's website and temporarily change his PC's IP to be in the same domain as the instrument, i.e. 172.16.xx.xx. Once the instrument's IP is successfully changed, the user can change back his PC's IP.

- It would be good if the user prints a label with the newly assigned IP address and sticks it on the instrument. If for some reason the IP is lost, the user will need to use the USB interface together with the ETHconfig software to "read" the IP.

Connect through Ethernet:

In order to connect via Ethernet, the IP address of the board is required. While no drivers are required; the user should simply know the current board IP address, and need to enter it in the text box next to the **IP** label, then click on the **connect** button.

The user can make sure that he is connected, by pinging the device.

To change the IP address of the board, the user needs to install the USB drivers.

(Refer to paragraph 11.3).

After installing the setup, the user will be able to open the ML4039B GUI.

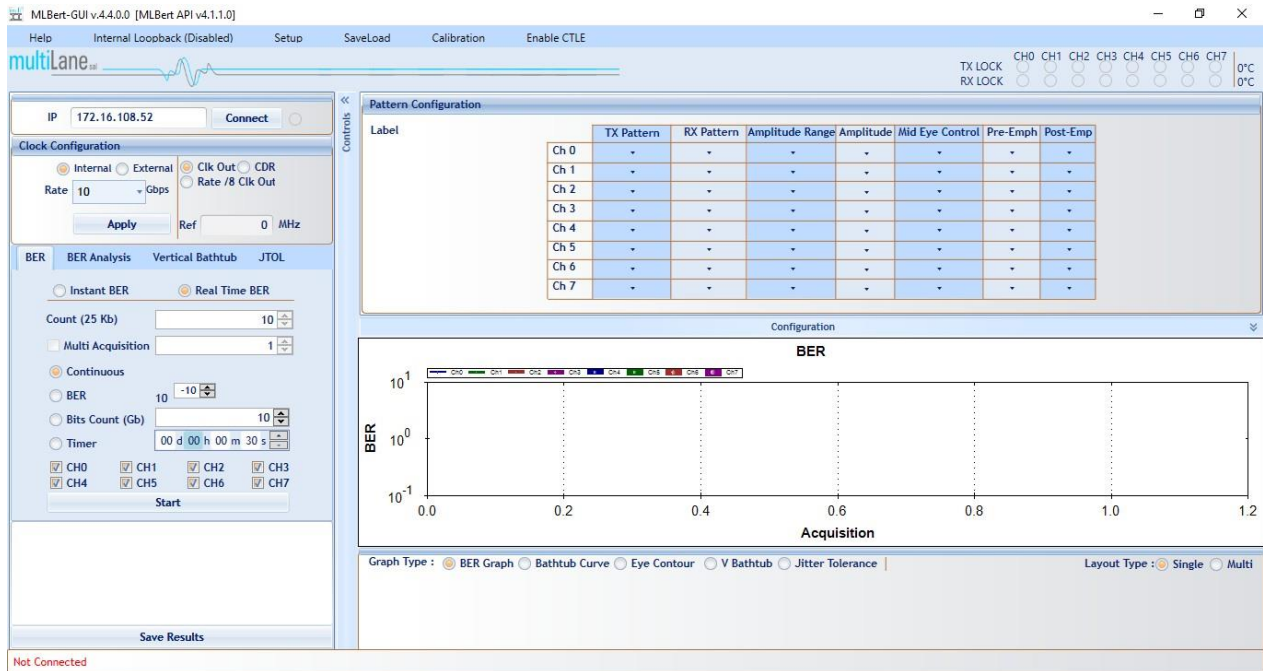


Figure 5: ML4039B GUI at start

11.3 Connecting Procedure

The user needs to connect using the board's IP, after that the board has been powered-up.



Figure 6: Connecting using the board IP

After clicking on Connect, all the Low voltage settings that have been saved during the calibration process are being applied. Also the last used configuration is being applied. Then the user can check the board's settings including the hardware ID and the firmware revision.

FWRev : 1.3 BoardID : 4644

Figure 7: ML4039B Firmware revision and Board ID

The displayed information is updated whenever any of the fields is being updated.

11.4 BERT Tab

At the first glance, after connecting to the board, the user will be able to detect on the GUI the: IP, Serial number, monitoring temperature, channels TX and RX lock, selected bit rate and all the clock configurations...

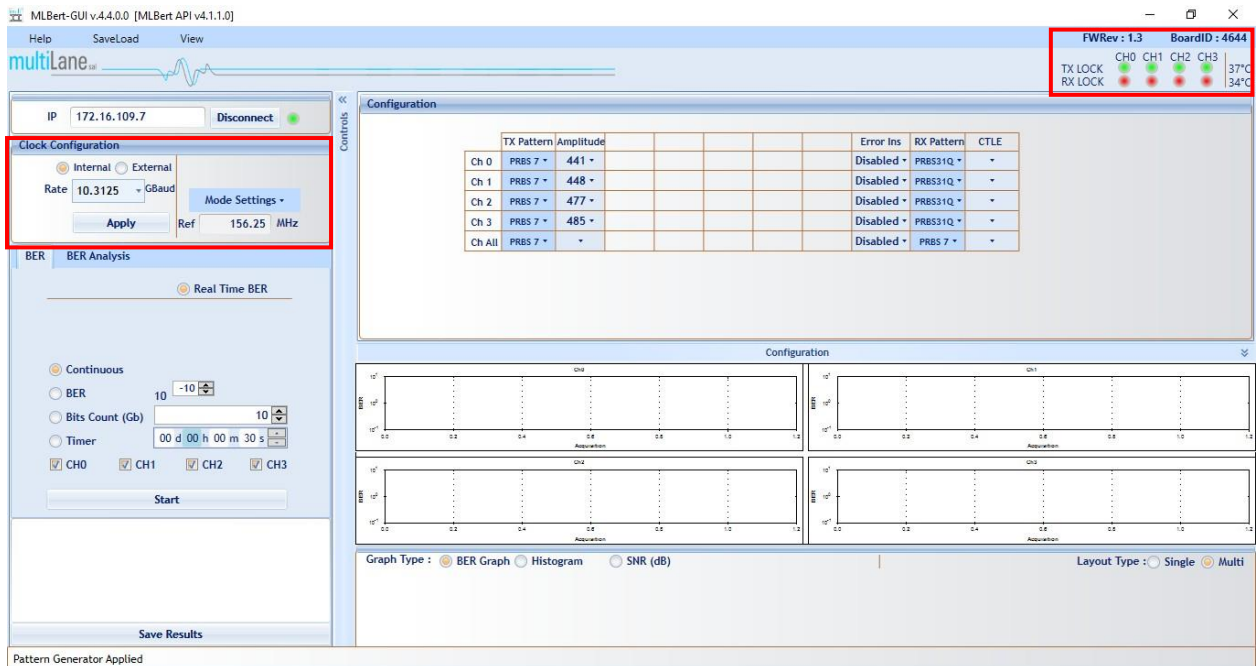


Figure 8: Main features detected after connecting

The user can select and control all the BERT settings.

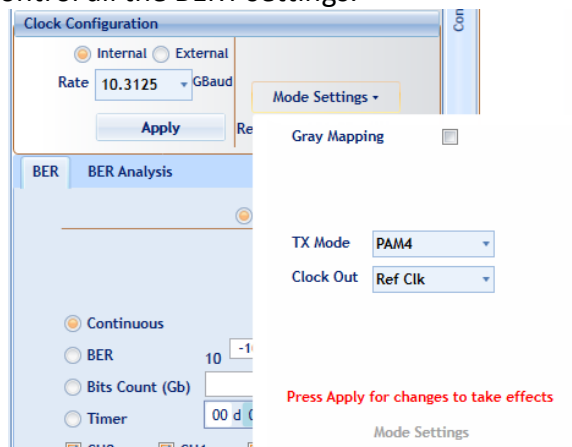


Figure 9: Rate and clock configurations

The ML4039B supports in low and high rates both eye modes: NRZ and PAM4.

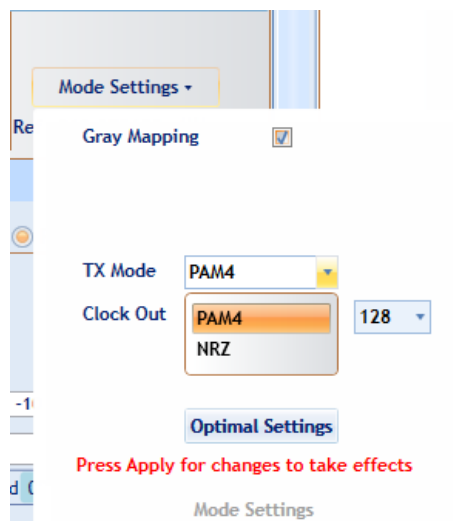


Figure 10: Supported eye modes

To switch between NRZ and PAM4 coding, use the TX Mode setting, then click Apply. The option Gray Mapping is only available in PAM4 mode. Gray Mapping enables use of PRBSxxQ defined in IEEE802.3bs. When Gray mapping is enabled, the PRBS13 and PRBS31 under the pattern select menu turn into PRBS13Q and PRBS31Q respectively.

For the clock source, the user can switch between clock-in and clock-out. Whenever any of the clock settings is changed the user should press apply.

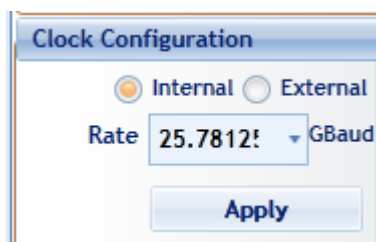


Figure 11: Clock options

If he selects external, which means that he is providing an external clock to the BERT, then he has to make sure the External clock is selected in the clock configuration **and** in the Mode Settings. The user should also press Apply and provide the appropriate clock input so the RX side of the BERT will be able to lock.

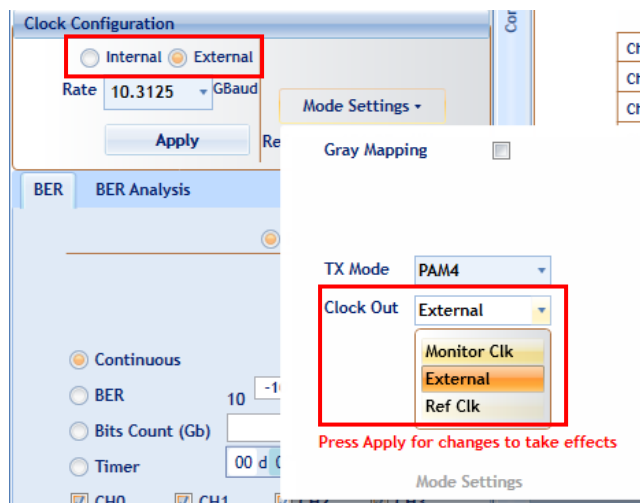


Figure 12: How to select external clock

For the clock-out available options, he has to first select internal. The user now can select from mode settings between reference clock and monitor clock. For optimal results the Ref Clk should be selected.

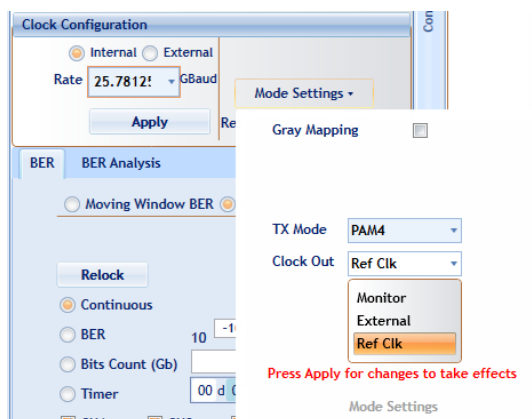


Figure 13: Internal Clock Selection

For the monitor clock the output can be controlled based on the selected clock divider.

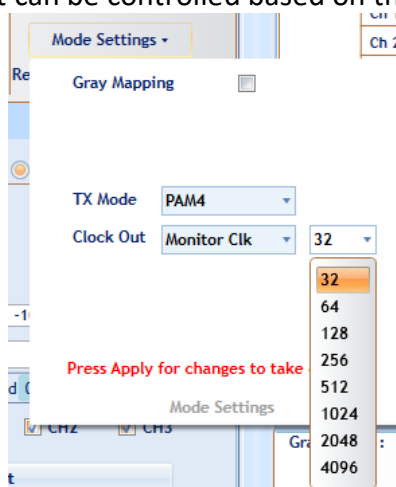


Figure 14: Monitor Clock-out options and dividers

For the line rate, the user can select any of the listed rates or he can enter any rate he wants, but this rate should be in the supported range as described in table 2.

The user can control all the BERT configurations, channel by channel.

The test can be run in Low voltage/ High Voltage settings mode (depending on the calibration applied) or in advanced mode.

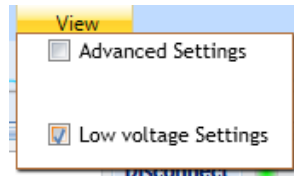


Figure 15: Selecting Advanced or Calibrated Settings mode

When operating in Low/ High voltage settings mode, the Low/ High voltage settings saved during the calibration process are being applied. And the user will be only able to control and change the amplitude. Based on the selected amplitude the software will automatically calculate the optimal settings.

Configuration										
	TX Pattern	Amplitude						Error Ins	RX Pattern	CTLE
Ch 0	PRBS 7 ▾	441 ▾						Disabled ▾	PRBS 7 ▾	▾
Ch 1	PRBS 7 ▾	448 ▾						Disabled ▾	PRBS 7 ▾	▾
Ch 2	PRBS 7 ▾	477 ▾						Disabled ▾	PRBS 7 ▾	▾
Ch 3	PRBS 7 ▾	485 ▾						Disabled ▾	PRBS 7 ▾	▾
Ch All	PRBS 7 ▾	▾						Disabled ▾	PRBS 7 ▾	▾

Figure 16: BERT side in Low Voltage settings mode

The ML4039B can output a wide range of pre-defined patterns. In addition to the PRBS patterns, there are linearity and jitter test patterns. Also, on top of the pre-defined patterns the user has the possibility of defining his own pattern.

Note: error detection only works on the PRBS patterns existing in the RX pattern drop down list. It is not possible to do error detection on custom defined patterns.

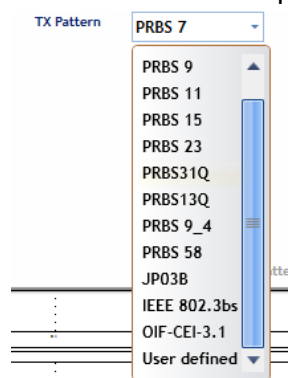


Figure 17: Pattern selection

In NRZ mode, for each level the corresponding eye amplitude is detected on the scope.

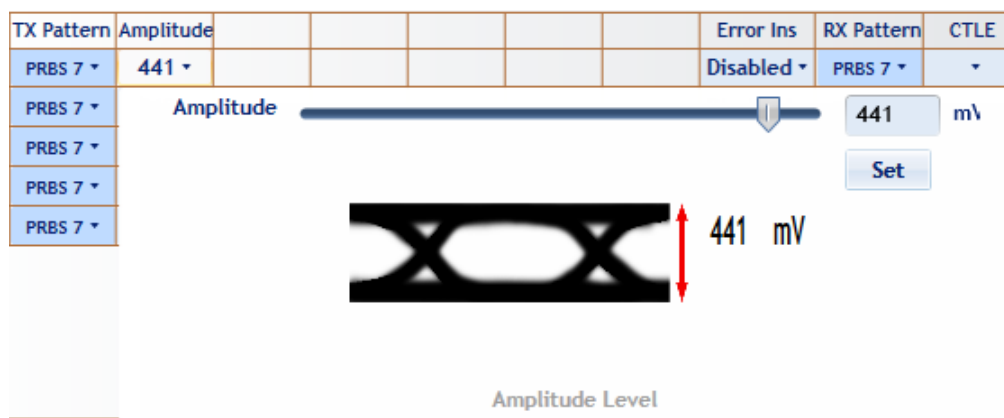


Figure 18: Amplitude control in NRZ mode and with the Low Voltage settings applied

In PAM4 mode, for each level the corresponding total eye amplitude is detected on the scope, this value is equal to the sum of the inner eye amplitude and two outer eye amplitudes. As shown in figure 19.

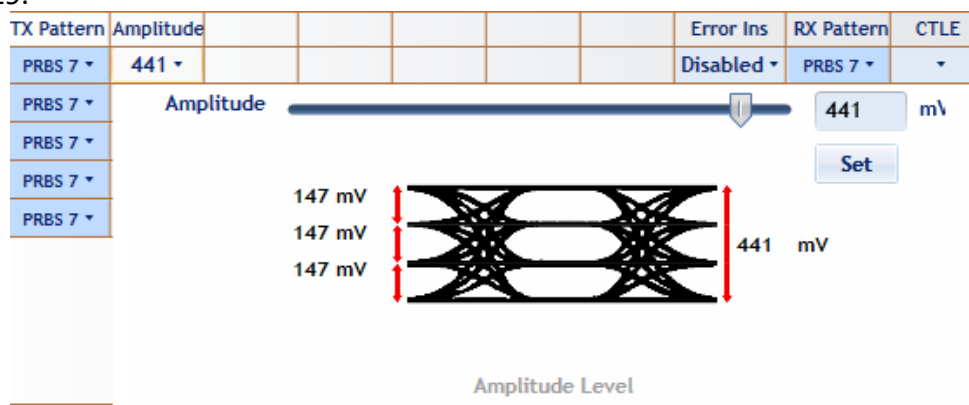


Figure 19: Amplitude control in PAM4 mode and with the Low Voltage settings applied

If the customer desires to control all the parameters, then he needs to go to the advanced mode. While switching between advanced settings and calibrated settings modes the user will be modified that the optimal settings are being applied.

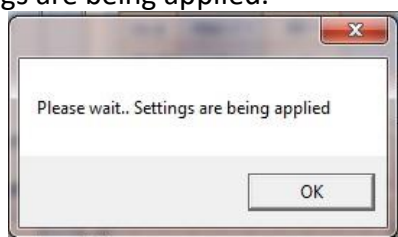
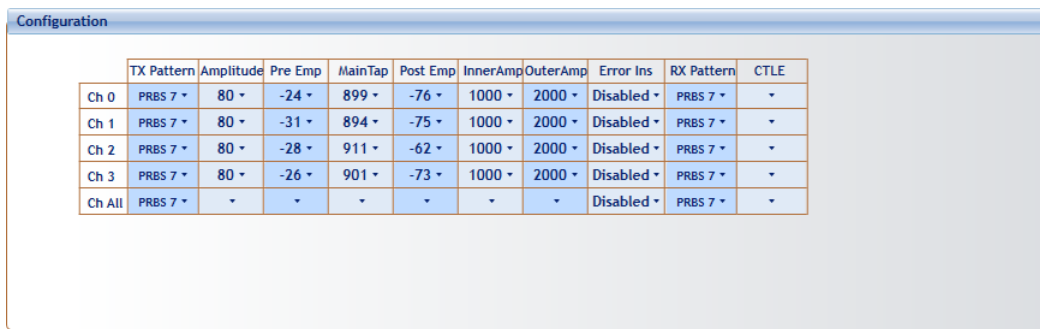


Figure 20: Settings being applied

If advanced settings mode is selected, after clicking "OK" on the pop-up window shown in figure 20, the BERT configuration window will be displayed as follows and the user will have access to control the amplitude and the FFE taps:



	TX Pattern	Amplitude	Pre Emp	MainTap	Post Emp	InnerAmp	OuterAmp	Error Ins	RX Pattern	CTLE
Ch 0	PRBS 7	80	-24	899	-76	1000	2000	Disabled	PRBS 7	
Ch 1	PRBS 7	80	-31	894	-75	1000	2000	Disabled	PRBS 7	
Ch 2	PRBS 7	80	-28	911	-62	1000	2000	Disabled	PRBS 7	
Ch 3	PRBS 7	80	-26	901	-73	1000	2000	Disabled	PRBS 7	
Ch All	PRBS 7							Disabled	PRBS 7	

Figure 21: BERT Configurations in PAM4 and Advanced Mode with 3 taps option

Main-Tap, Pre and Post Emphasis level varies between ± 1000 . The amplitude slider does not show anymore the values that have been saved during the calibration. The user can go up to 120% and the corresponding amplitude is detected on a scope.

To access the 7 taps FIR the user should select the advanced settings then go to the mode settings tab and enable the 7 taps option, and press apply.

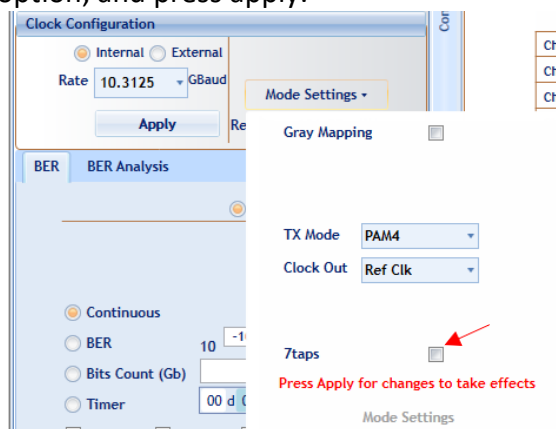
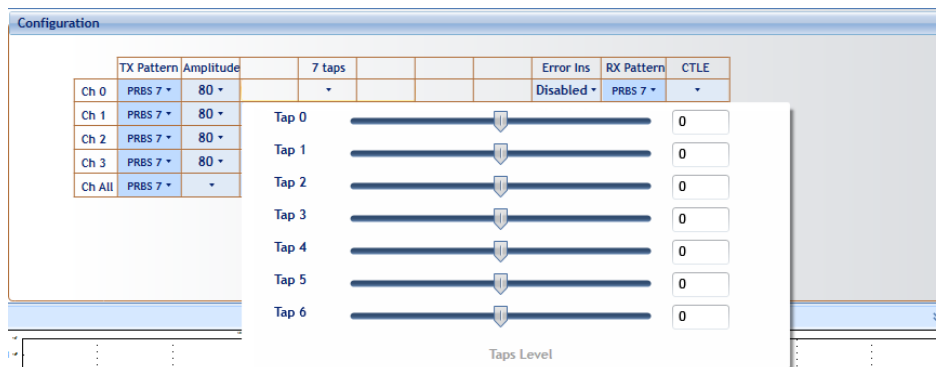


Figure 22: Enabling the 7 taps FIR option



	TX Pattern	Amplitude	7 taps	Error Ins	RX Pattern	CTLE
Ch 0	PRBS 7	80		Disabled	PRBS 7	
Ch 1	PRBS 7	80				
Ch 2	PRBS 7	80				
Ch 3	PRBS 7	80				
Ch All	PRBS 7					

Tap	Level
Tap 0	0
Tap 1	0
Tap 2	0
Tap 3	0
Tap 4	0
Tap 5	0
Tap 6	0

Figure 23: Configurations Tab in PAM4 and Advanced Mode with 7 taps option

The user can test the BER, histogram and SNR, on the selected channels.

Error insertion can be controlled channel by channel.

All these measurements can be performed on all the rates, patterns and in NRZ and PAM4 modes. Below are shown some screenshots showing the eye in PAM4 and NRZ modes using to the MLDSO. These screenshots are captured, with the 80% calibrated settings (low voltage) being applied.

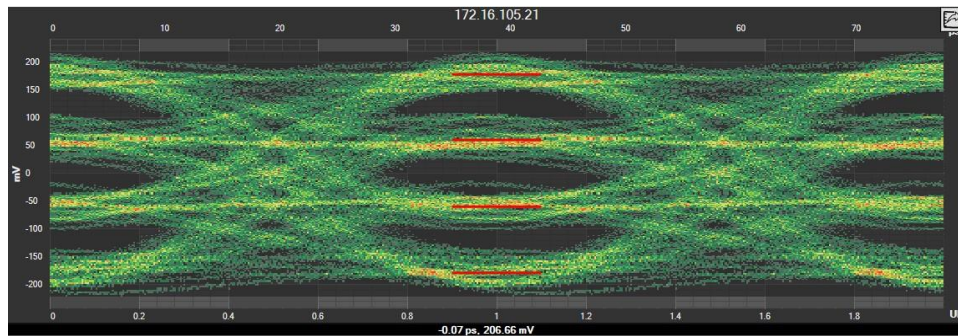


Figure 24: PAM4 mode, high rate

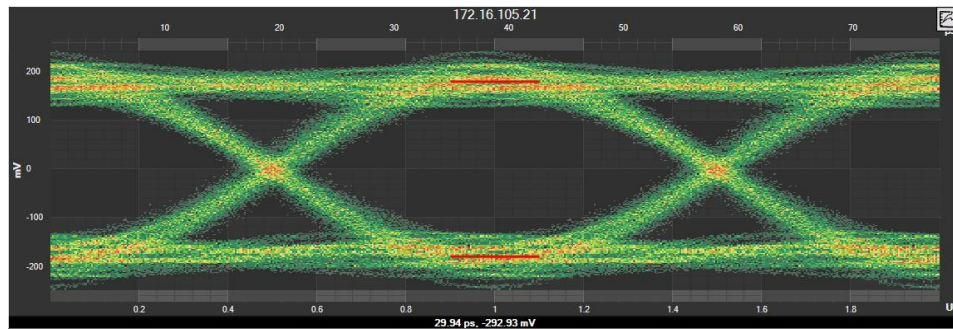


Figure 25: NRZ mode, high rate

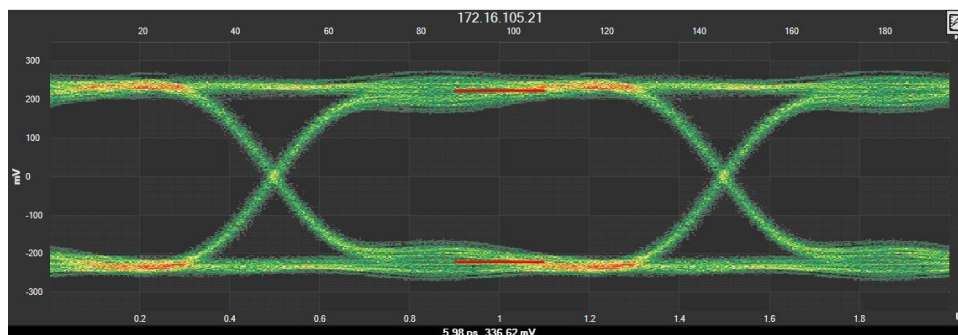


Figure 26: NRZ mode, low rate

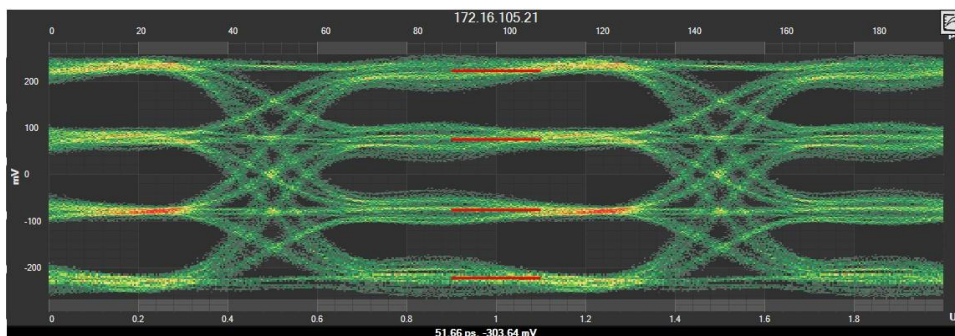


Figure 27: PAM4 mode, Low rate

11.5 BERT measurements

To be able to start BER measurements, the instrument ports should be in the loopback mode, which means the TX ports should be connected to the RX ports and the PPG and ED patterns should match. It is not necessarily to supply a PRBS from the same physical instrument – the source can be a different instrument and the error-detector of the ML4039B can derive its own clock from the received data (no need for a separate clock link). However, if Gray coding is used in the source, one should tell the receiver to expect Gray coding as well. There should be a match in pattern, polarity and coding to have lock. If an external clock source is used, then the clock value should be equal to the value of the reference clock.

The user can run the BER test on selected channels continuously or choose a target BER or set a timer.

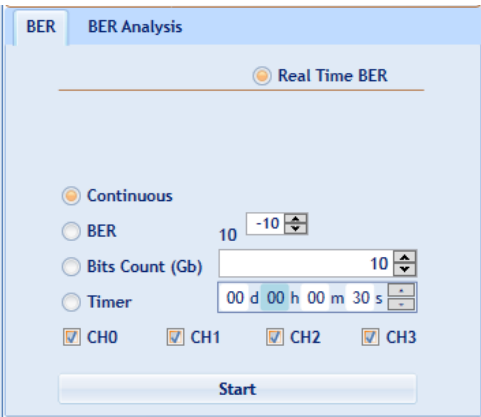


Figure 28: BER control panel

The BER values are displayed per channel and their corresponding BER graph. The graph shows the total BER value.

	BER	Error Count
Ch1	0.00e+00	0.00e+00
Ch2	0.00e+00	0.00e+00
Ch3	0.00e+00	0.00e+00
Ch4	0.00e+00	0.00e+00

Save Results

Figure 29: BER values in NRZ mode

Ch1	
Error Count	0.00e+00
BER	0.00e+00
Ch2	
Error Count	0.00e+00
BER	0.00e+00
Ch3	
Error Count	0.00e+00

Save Results

Figure 30: BER values in PAM4 mode

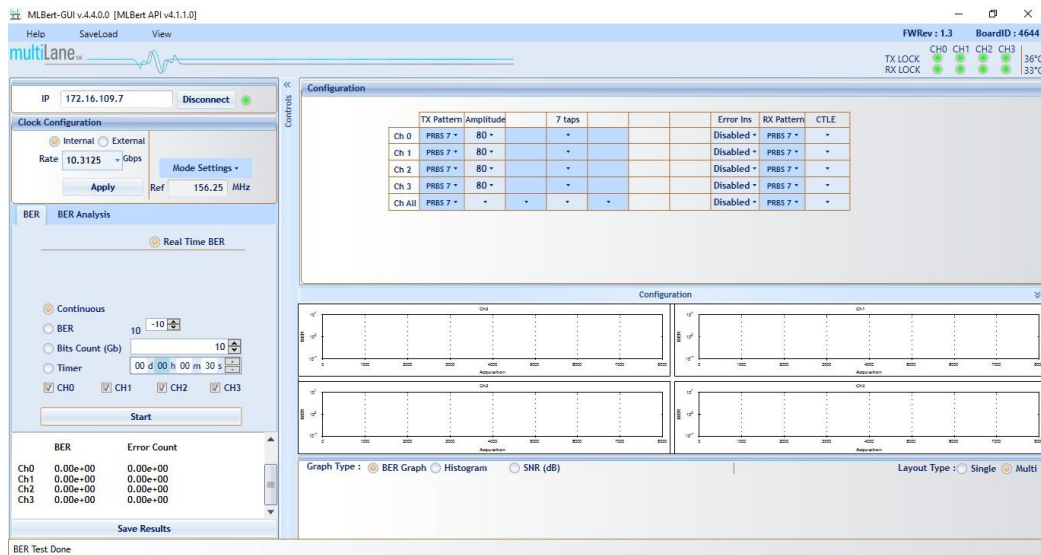


Figure 31: BER test on 4 channels

The user can test the BER, histogram and SNR, on the selected channel, in NRZ and PAM4 modes.

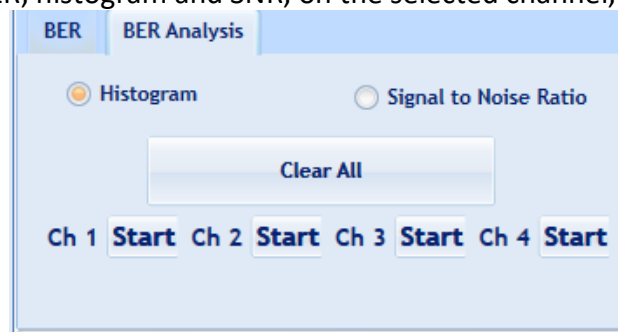


Figure 32: BER analysis tab

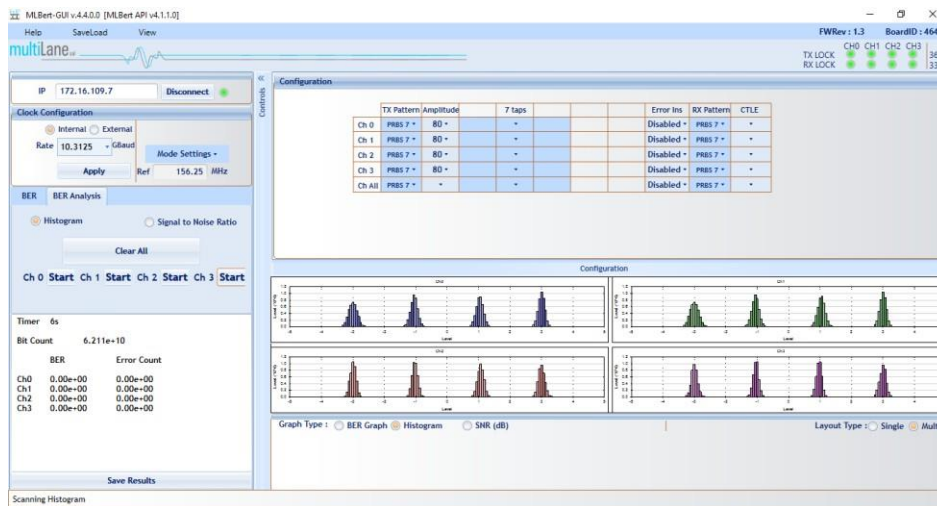


Figure 33: Histograms in PAM4 mode

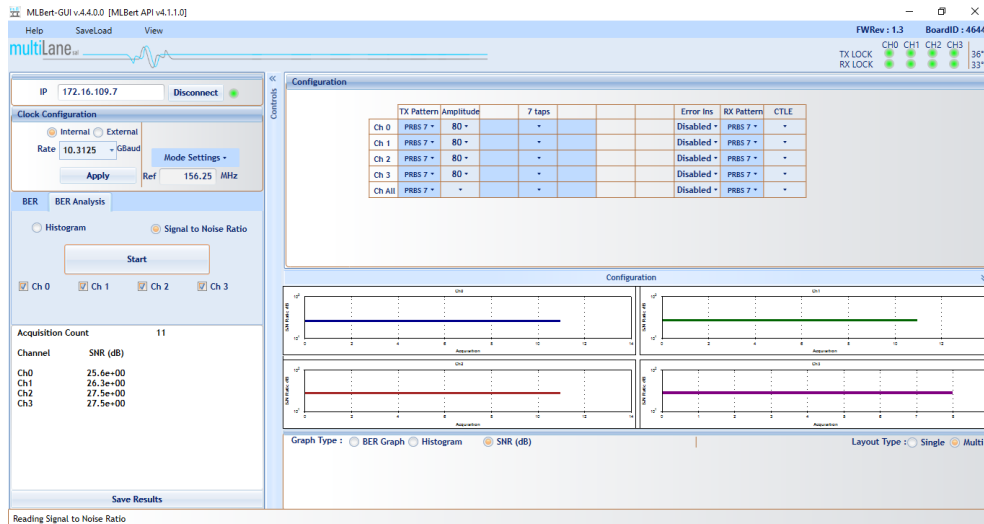


Figure 34: SNR in PAM4 mode

This BERT gives the user the possibility to insert errors by enabling the error insertion option.

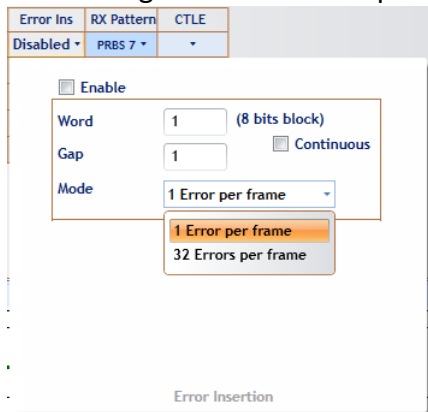


Figure 35: Error Insertion options in NRZ mode

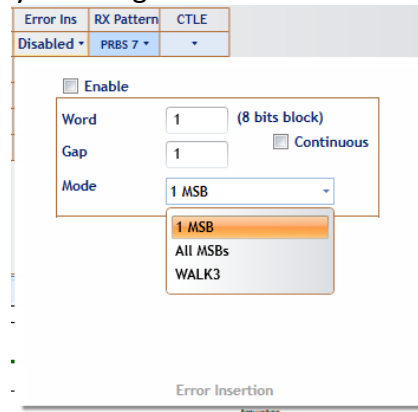


Figure 36: Error insertion options in PAM4 mode

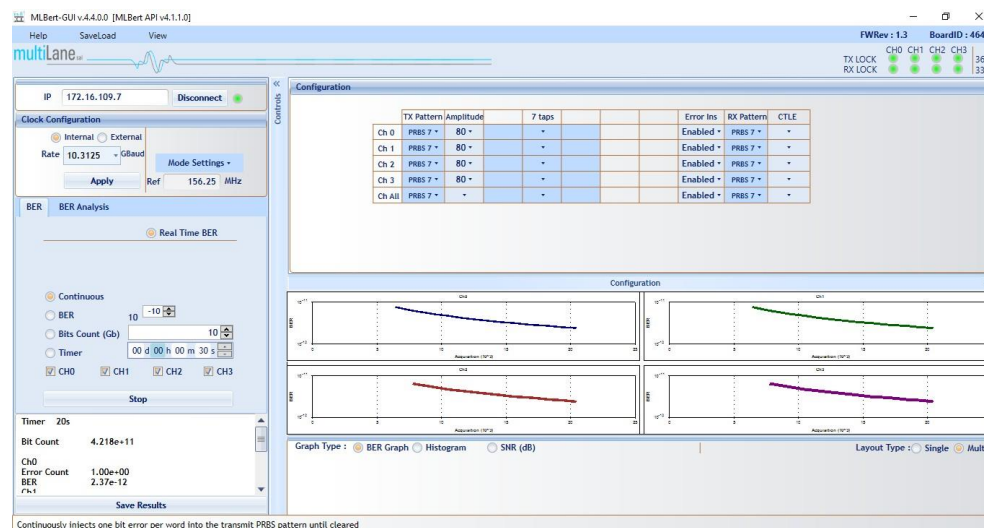


Figure 37: BER measurement with 1 error inserted at the MSB

The user can choose among two DSP modes: slicer for non-strenuous links and slicer with reflection canceller also the user can change CTLE values using the slider.

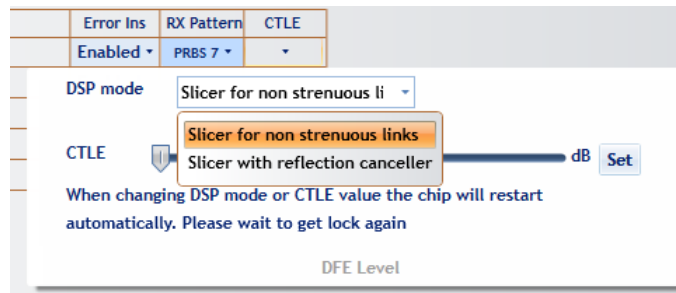


Figure 38: DSP mode options and CTLE slider

12. IP changer tool

If the user needs to change the IP of the board, the link represented below, has all needed tools (software and user guide).

<https://multilaneinc.com/berts-gui/>



Setup MLIPChanger-v12



ML IP Changer Guide V 11



ML4039-eth-configuration-software

Figure 39: IP changer GUI and User Guide

Figure 40: Ethernet Configuration Software

13. Revision History

Revision number	Date	Description
1.0	11/14/2019	▪ Document created

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