

MultiLane and Yamaichi Demonstrate 802.3ck Interconnect Solutions With 100G-Per-Lane Signal Transmission

Wednesday, April 6th, 2022

SANTA CLARA, Calif. – With the steady increase of 5G network demand and deployment, the need for high-speed data transmission on network equipment such as routers and switches continue to increase. To meet this market demand, MultiLane (booth #1155) and Yamaichi (booth #960) have collaborated to showcase new interconnect solutions capable of transmitting 100G per electrical lane in a live demonstration at DesignCon 2022.

The next frontier of cloud-scale connectivity is being addressed by Yamaichi with innovations such as the "Jumper" Cable Interconnect and QSFP-DD800 Connector solutions. The demo is supported by 4x100G test solutions provided by MultiLane. The combination of the ML4039E 4x100G Bit Error Rate Tester (BERT) and ML4015D-E Digital Sampling Scope (DSO) comprise a proven test setup to showcase the high signal fidelity and maturity of multiple Yamaichi interconnect products.

"We are excited to be collaborating with Yamaichi to showcase their 100G-per-lane interconnect solutions with our state-of-the-art equipment", said Elias Khoury, Product Line Manager at MultiLane. "We aim to enable the deployment of such game-changing interconnect innovations by providing the necessary means for performance and reliability validation." The combination of the MultiLane DSO and BERT enable both time and frequency domain measurements such as insertion loss (SDD21), PAM4 eye diagram, and real-time bit-error-rate (BER), crucial performance metrics for high-speed cables and interconnects. With a mix of unique BERT features like multi-tap transmitter equalization and a rich suite of software filters, signal characterization and analysis become highly intuitive tasks.

These MultiLane instruments can be seen driving two novel interconnect solutions at the Yamaichi booth at DesignCon. First, a mated 800G compliance fixture (Module Compliance Board and Host Compliance Board) with the Yamaichi QSFP-DD800 connector displays BER performance with significant margin. Second, a full-rate signal is driven through a Yamaichi 100G-per-lane jumper cable and OSFP112 connector/cage, ending with a PAM4 eye capture via the MultiLane DSO. "Yamaichi strives to develop leading-performance connectors, sockets and cable solutions which enable new standards like 800G Ethernet", said Takeshi Nishimura, Director and Business Unit Manager at Yamaichi Electronics USA. "We highly value this partnership with MultiLane which proves the maturity of our 100G-per-lane product families to our mutual customers." Yamaichi and MultiLane have commenced further performance enhancement studies towards next-generation technologies like 200/224Gbps per electrical lane.

About MultiLane:

MultiLane Inc. is a leading provider of High-Speed IO and Data Center Interconnect test solutions from 10G to 800G. Products include BERTs, TDR, optical and electrical oscilloscopes, optical switch boxes, CMIS testers, and a host of MSA-compliant development tools for QSFP28, QSFP-DD, OSFP, and other standards. MultiLane solutions are used to test semiconductors, DACs, AOCs, active cables, optical transceivers, and system switch cards. MultiLane also offers compliance and interoperability test services along with high-speed design consultation and development services.

About Yamaichi Electronics:

Yamaichi Electronics is a global provider of interconnect solutions for customers in the telecommunications, datacom, automotive, medical, industrial, and semiconductor test/burn-in markets. Providing stable and high-performance interconnect solutions for numerous mission-critical situations has earned the company a renowned reputation among top tier telecom and datacom customers over the last decade. Yamaichi Electronics is expanding its connector product lineup for front pluggable module form factors such as QSFP, QSFP-DD, SFP, SFP-DD, DSFP, OSFP, CFP, CFP2, CFP4, and CFP8, as well as high pin count mezzanine board connectors and jumper cable assembly for chip-to-chip and chip-to-I/O applications, to 100G per lane signal transmission in 2022.

 [LinkedIn](#)

 [Facebook](#)

 [TWITTER](#)

 [YouTube](#)

 [Website](#)