Leiurus: MultiLane’s Probing Solution
TDR Probing & PCB Failure Analysis

Elias Khoury
1/22/2021
Outline

- **Background** – The Status-Quo
- **Leiurus** – TDR Probing Solution
  - Setup & Hardware
  - Probes
  - Key Measurements
  - Applications
- **ML4035** – The Swiss Army Knife of Signal Integrity
- **ML4035 Technical Specs** – PPG, ED, DSO
Background
The Status Quo

- PCBs and connectors make up the core of high-speed systems and their reliable performance is crucial for successful operation.
- The imbalanced growth between speed and innovative testing solutions is driving test time, complexity and cost to new heights.
- MultiLane’s goal is to provide a fast, reliable and affordable alternative to traditional testing methods, allowing PCB & connector users and manufacturers to ensure reliable operation of their products.
Leiurus

TDR Probing & PCB Failure Analysis

- MultiLane’s solutions cover the whole spectrum of the industry’s testing needs including evaluation of the smallest, most delicate, and hardest traces to reach.

- MultiLane has combined its state-of-the-art technology in its ML4035 with the high quality DVT Solutions probes to provide a comprehensive TDR probe testing solution for PCB & interconnects.
Leiurus

Setup & Hardware

- ML4035
- DVT40/DVT-FP70
- DVT-FP250 Probe Positioner
- DVT-FP100 Magnetic Bases
- DVT-CS1/5 Camera System
Leiurus

Probes

- DVT40 (40 GHz) or DVT-FP70 (40/50/70 GHz)
- Single-ended & true odd mode differential probes with variable pitch.
- Conductive diamond & gold-plated probe tips
- Can measure single-ended & differential traces that have no ground access.
- Minimum TDR rise-time degradation
- Repeatable TDR measurements
Leiurus

Key Measurements

- Impedance Profile
- Insertion Loss
- Return Loss
- Crosstalk
- Eye Diagram
- Bit Error Rate
Leiurus

Applications

- Failure Analysis
- Impedance Matching
- Trace Verification
- Motherboard/daughter cards
- Chip-to-module electrical channels
**ML4035: Swiss Army Knife of SI**

**Key Features**

- 4-Lane Sampling Scope
- 4-Lane 53GBd PPG
- 4-Lane True-Differential TDR/TDT
- 400G Bit Error Ratio Tester
- Automation SW for DAC Testing
- High Throughput

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Clk In/Out</td>
<td>The trigger input for the sampling scope (DSO). It is used in DSO mode only.</td>
</tr>
<tr>
<td>2 CH1 - CH4</td>
<td>TDR/DSO ports. Each channel can be either configured as TX or RX.</td>
</tr>
<tr>
<td>3 TX1 – TX4</td>
<td>PPG ports. Each channel can transmit a 53 GBd NRZ/PAM4 signal.</td>
</tr>
<tr>
<td>4 RX1 – RX4</td>
<td>Error Detector ports. Used to measure BER.</td>
</tr>
<tr>
<td>5 LAN</td>
<td>RJ-45 port for data transfer and communication with the GUI</td>
</tr>
</tbody>
</table>

Innovation for the next generation
BERT Specs

PPG Features

- PAM-4: 22 – 29.6 and 48 – 56 GBd
- NRZ: 22 – 29 and 48 – 56 Gbps
- DFE Pre-coding and Gray coding
- Channel Emulation & Full FEC
- PRBS7/9/11/13/15/16/23/31/58  PRBS13Q, 31Q and SSPRQ Square wave,  JP03A/B,  CID JTOL pattern
- Maximum voltage swing: 0 – 800 mVpp
- Pre and Post-emphasis

ED Features

- Total DFE/FFE/CTLE equalization up to 13 dB
- SNR monitoring
- FEC measurements
- PAM4 slicer threshold adjustable
- Reference clock output rate div 8/16/32/165
- PRBS 7, 9, 13, 15, 23 & 31 checker
- Automatic PRBS detection
- Clock-data recovery
- BER counters
- Error insertion
DSO Specs

- 4-Lane 35 GHz Digital Sampling Scope optimized for high-speed data analysis
- High fidelity signal capture
- Low intrinsic Jitter
- Jitter decomposition (TJ, RJ, DJ)
- CTLE, S2P De-embedding, FFE, DFE, etc...
- SSPRQ & up to PRBS16 pattern lock
- NRZ and PAM measurement Libraries (APIs)

TDR Specs

- High resolution TDR/TDT measurements
- 4-Lane 35 GHz Time Domain Reflectometry / Transmission optimized for high-speed tests and measurements
- Impedance profile measurement
- S-Parameters:
  - Return & Insertion loss
  - Crosstalk
  - Accurate multisport S-parameters