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BROCHURE

Innovation for the next generation

V93000 HSIO High-Speed Solution

32 bidirectional differential Lane Count | BERT and DSO, Source/Measure up to 112 Gbps | NRZ and PAM4 | SmarTest API's | V93000 production ready| Loadboard accessories

Summary

MultiLane has ported its leading-edge high-speed benchtop BERT and scope DSO technologies into Advantest's V93000 ATE tester to expand digital and analog validation and production testing capabilities. The fully integrated BERT and DSO instruments provide testing capabilities of 32 lanes at up to 112 Gbps (PAM4) and 50 GHz input bandwidth. V93000 Smartest software and hard docking solutions are already deployed worldwide, with proven reliable results in a production environment.

This unique setup enables testing of packaged silicon as well as wafer probe, including at-speed testing of SerDes, transceivers, amplifiers, ASICs with high-speed I/O, and other active and passive high-speed devices. Testing is accomplished at the PHY level for Ethernet, HDMI 2, USB 3/4, PCIe 5/6, Fiber-Channel and others. The BERTs and Scopes can also be used for IC validation, characterization, and production testing.

In addition, MultiLane offers ATE-related services including DUT load board design, and signal integrity simulation.

V93000 HSIO System Overview

Advantest and MultiLane offer a single platform solution which leverages the best capabilities and qualities of both companies. The BERTs and DSOs are located directly under the load board, in the cavity of the test head extender called the Twinning Frame. Due to this proximity to the load board, the signal path from BERT/DSO to the DUT is extremely short. This significantly enhances signal integrity and test accuracy.

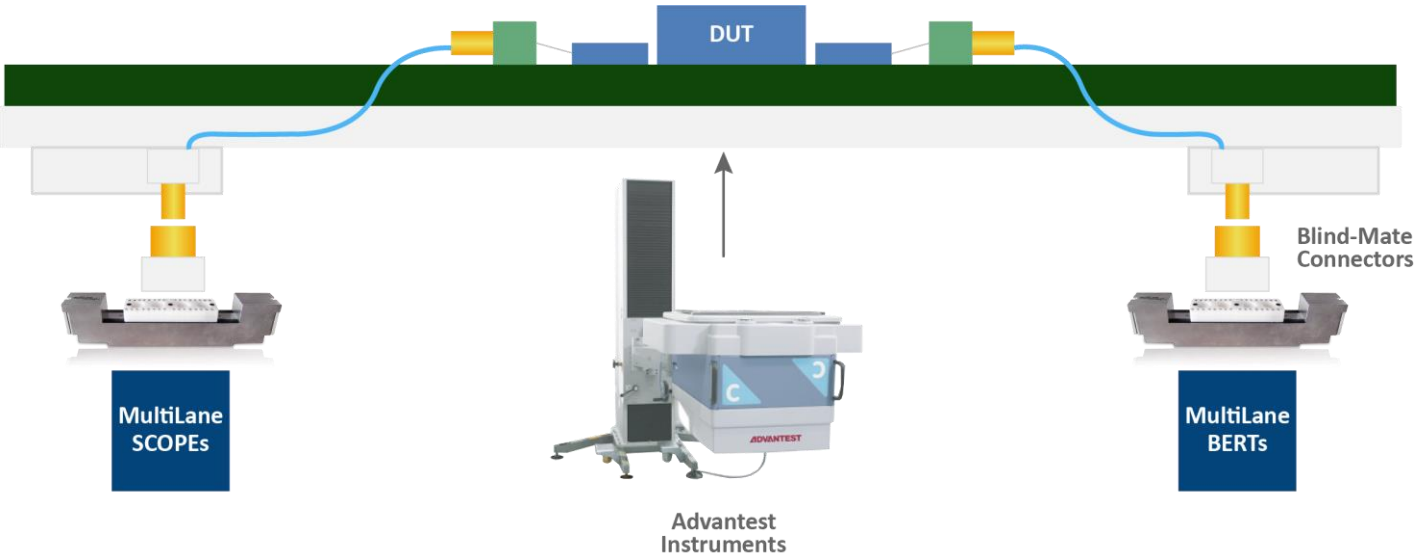

Figure 1: Overview of the V93000 HSIO System

Figure 2: Twinning Frame with MultiLane BERTs and DSOs inside.

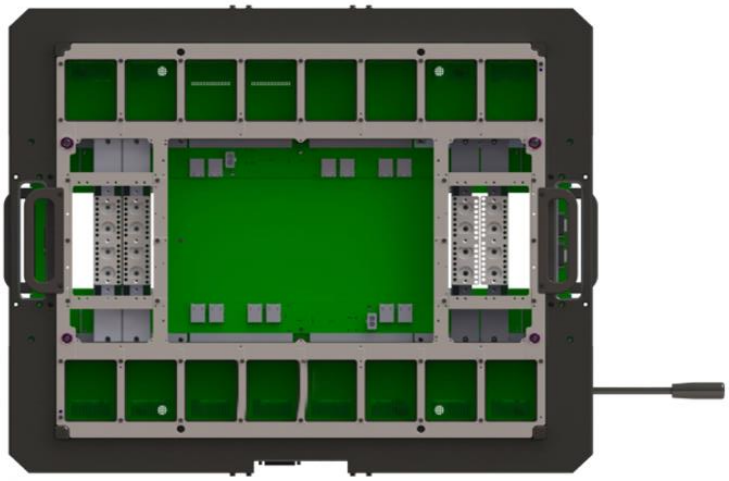

Figure 3: Four HSIO MultiLane cassettes mounted inside a twinning frame.

Key Features and Benefits

Key Features

- 32 synchronized lane testing
- NRZ & PAM4 signals
- Blindmate RF cable connection
- V93000 Smartest Software API's
- Multisite ready software
- Direct Docking
- At-Speed Wafer sort testing
- At-Speed Package testing
- Easy movement of capabilities between bench and ATE

Key Benefits

- High-speed interface testing
- Complementary testing capabilities to the V93000 test platform
- BERTs and SCOPEs compensate for cable and DUT board traces
- SmarTest tools help speed test program development and multisite deployment
- Advantest docking allows quick and reliable interfacing to a wide variety of device handlers and wafer probers

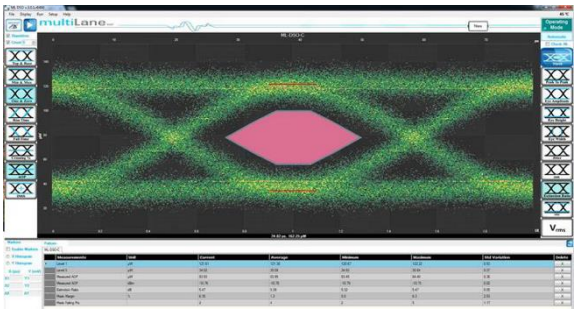

Figure 4: NRZ Eye Measurements

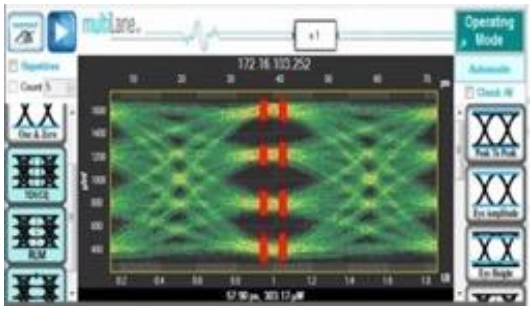

Figure 7: PAM4 Eye Measurements

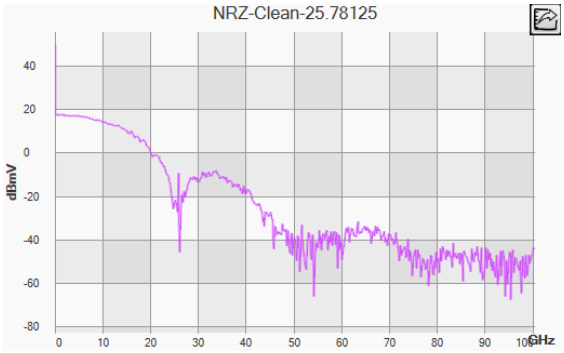

Figure 5: Measuring Total Harmonic Distortion

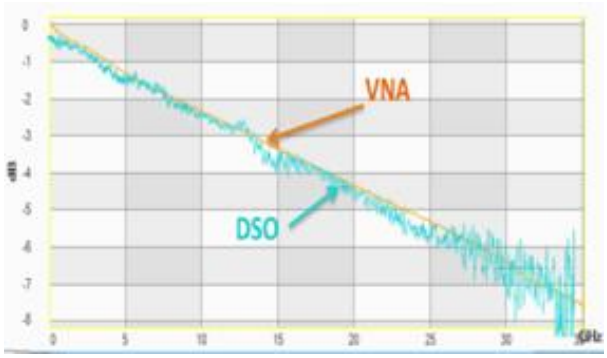

Figure 8: Correlated S21 measured - VNA and DSO

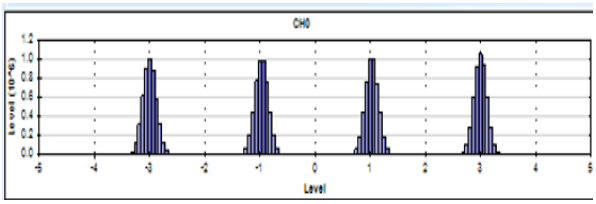

Figure 6: BERT PAM4 eye histogram

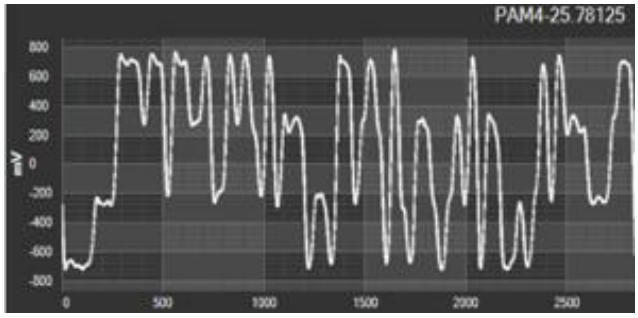

Figure 9: PAM4 signaling measured on DSO

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Instruments Specs

50 GHz Electrical DSO (AT4025-50)

DSO Features

- 50 GHz input bandwidth
- Fast sampling and DSP using optimized hardware and Smartest software
- Extensive library of built-in DSP filters such as Bessel-Thomson, CTLE, DFE, FFE, de-embedding and component emulation
- De-embedding tools to compensate for insertion losses that are always present in high-speed signaling
- Built-in standard masks library
- A complete set of APIs and multiple SmarTest sample code to speed up integration.

4-Lane BERT 28 GBd PAM4/NRZ (AT4039D)

Programmable Pattern Generator Features

- High-speed clock out to 3 GHz
- Gray coding, polarity inversion
- PRBS7, 9, 13, 15 23, 31, 58
- PRBS13Q, 15Q, 31Q
- Up to 1500 mVppd voltage swing
- Patterns are generated algorithmically
- Custom patterns: 64 bits can be repeated up to 255 times and repeated as needed

Error Detection Features

- FFE Equalizers
- > 13 dB equalization with FFE+CTLE
- PAM4 eye balance tuning
- Eye contour and PAM level histogram
- PRBS7, 9, 13, 15, 23 & 31 checker
- Automatic PRBS detection

4-Lane BERT 56 GBd PAM4/NRZ (AT4039E)

PPG Features

- High-speed clock out to 7 GHz
- Real FEC and Gray coding
- PRBS7, 9, 13, 15, 23, 31, 58
- PRBS13Q, 31Q
- Up to 800 mVppd voltage swing
- Patterns are generated algorithmically
- Custom patterns: 64 bits can be repeated up to 255 times and repeated as needed

Error Detection Features

- FFE Equalizers with reflection cancellation and DFE
- PAM4 eye balance tuning
- Eye contour and PAM level histogram
- PRBS7, 9, 13, 15, 23 & 31 checker
- Automatic PRBS detection
- Clock-data recover
- BER counters

4-Lane SE BERT 56 GBd PAM4/NRZ With EML Driver (AT4039EML)

PPG Features

- High-speed clock out to 7 GHz
- Real FEC and Gray coding
- PRBS7, 9, 13, 15, 23, 31, 58
- PRBS13Q, 31Q
- Up to 1800 mVppd voltage swing
- Single-ended high swing EML output driver

ED Features

- FFE Equalizers with reflection cancellation and DFE
- PAM4 eye balance tuning
- Eye contour and PAM level histogram
- PRBS7, 9, 13, 15, 23 & 31 checker

8-Lane 1 – 28 GBd PAM4/NRZ (AT4079B)

Key Features

- Low-cost alternative to higher-speed and higher-swing 4-lane BERTs
- Instrument-grade BERT optimized for high-speed data analysis of 100G/200G/400G transceivers
- Ability to tune the bit rate in very fine steps to facilitate finding the locking margin.
- FEC support
- Supports PRBS13Q/15Q/31Q and user-defined patterns
- API library, sample code and Python wrapper

4-Lane BERT 28 GBd NRZ with Jitter Injection (AT4039B-JIT)

Key Features

- Bitrate coverage 1 – 30 Gbps continuous
- Sinusoidal Jitter Modulation to 100 ps
- Phase skew adjustment to +/- 50 ps
- Random jitter injection
- Random interference injection
- Error insertion
- User defined pattern generation
- Supports all standard PRBS patterns

SmarTest Software

V93000 Control

- MultiLane API's for Advantest Smartest 7.x
- Multisite Testing
- Full use of all Advantest related Smartest software features
- BERT and DSO sample code provided
- High throughput multithreaded DSP routines
- Linux RHEL5 and RHEL7
- Via Ethernet

Windows based control

- Alternative path into MultiLane instruments using laptop control
- Via Ethernet

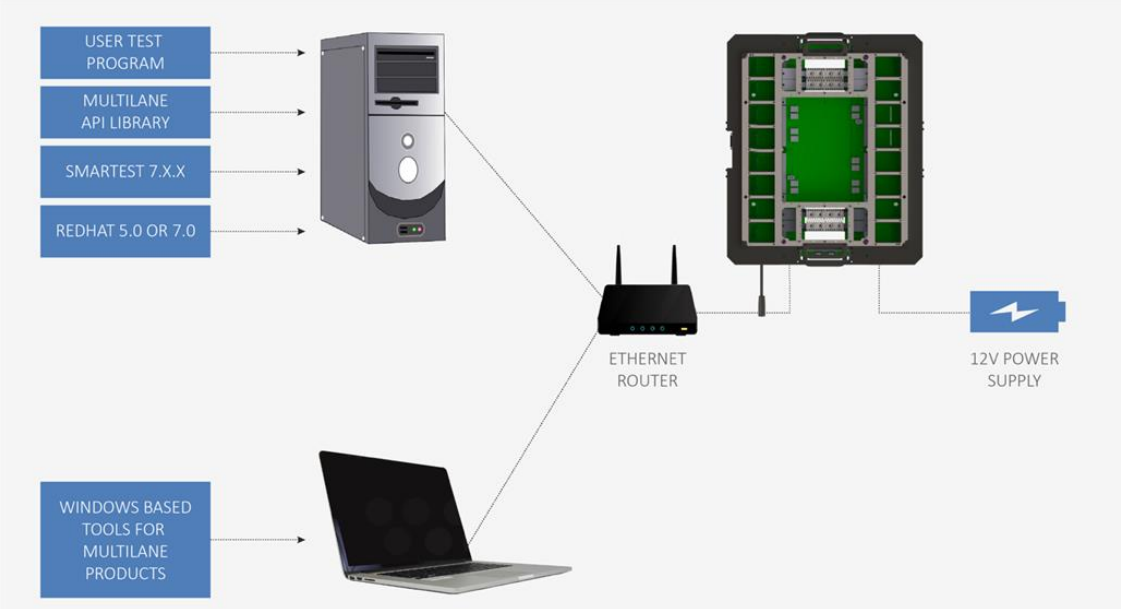

Figure 10: SmarTest Integration Model

Ordering Information

Details	Product Number
4-channel 50 GHz Bandwidth Digital Sampling Oscilloscope. ½ cassette	**AT4025**
4-lane 56 Gbps (28 GBaud PAM4/NRZ) BERT. ½-cassette	**AT4039D**
4-lane 112 Gbps (56 GBaud PAM4/NRZ) BERT. ½-cassette	**AT4039E**
4-lane 112 Gbps (56 GBaud PAM4/NRZ) BERT with single-ended high-amplitude outputs for driving EMLs. ½ cassette	**AT4039EML**
8-Lane 60 Gbps (30 GBd PAM4/NRZ) BERT. 1-cassette	**AT4079B**
4-Lane 30 GBd NRZ - BERT with Jitter Injection. 1-cassette	**AT4039B-JIT**
Twinning Frame infrastructure	**Contact MultiLane**
Package Test and Wafer Probe Test Loadboard Accessories	**Contact MultiLane**
Specialized high-speed cable assemblies	**Contact MultiLane**
ATE-related services including DUT load board design, and signal integrity simulation	**Contact MultiLane**

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